2020 LithoVision

Economics in the 3D Era

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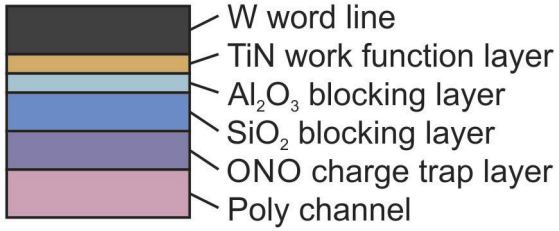
Outline

- Discuss the three main industry segments that drive the state-of-the-art:
  - 3D NAND
  - Logic
  - DRAM
- For each segment present current status, roadmaps with technology, and resulting mask counts, transistor or bit density and transistor or bit cost trends.
- Conclusion

3D NAND TCAT Process

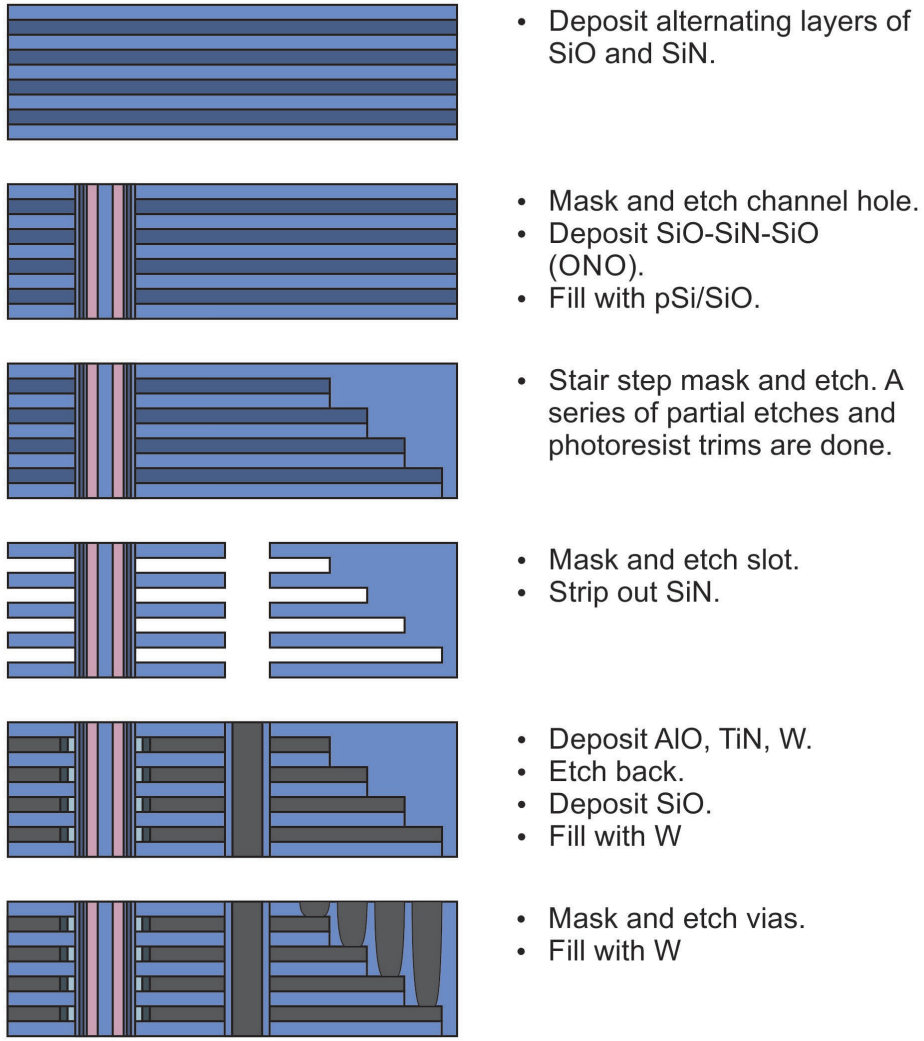
1. CMOS fabrication
2. Memory array formation – single string or string stacking. String stacking repeats layer deposition, channel and stair step formation and adds an etch stop layer with channel feedthrough.
3. Interconnect



Charge trap cell (Samsung/Kioxia)

Memory array masks

- Channel mask
- Multiple stair step masks depending on the number of layers
- 1 or 2 slot masks
- Via mask
- Clear out masks



Memory array string formation (Samsung/Kioxia)

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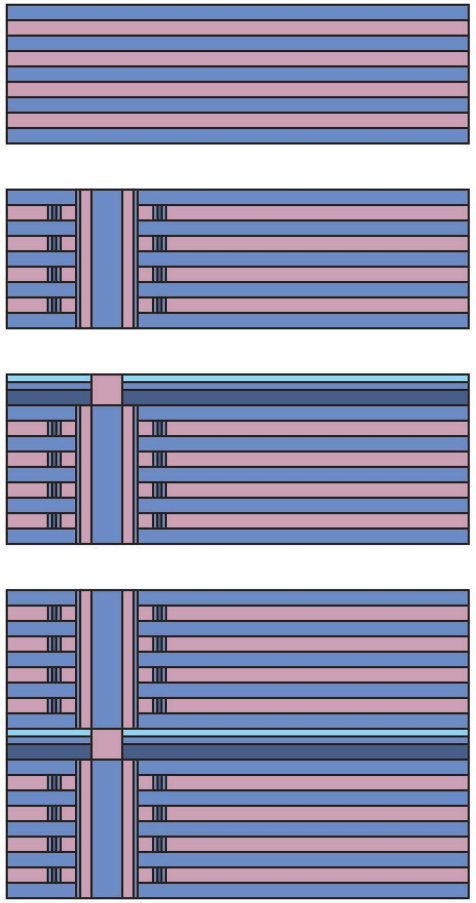
Intel-Micron String Stacking

- Due to the difficulty of etching oxide-polysilicon pairs Intel-Micron is the first company to string stack.
- String stacking splits up the memory array stack formation into strings.
- This simplifies the channel hole formation – the channel hole is the highest aspect ratio feature.

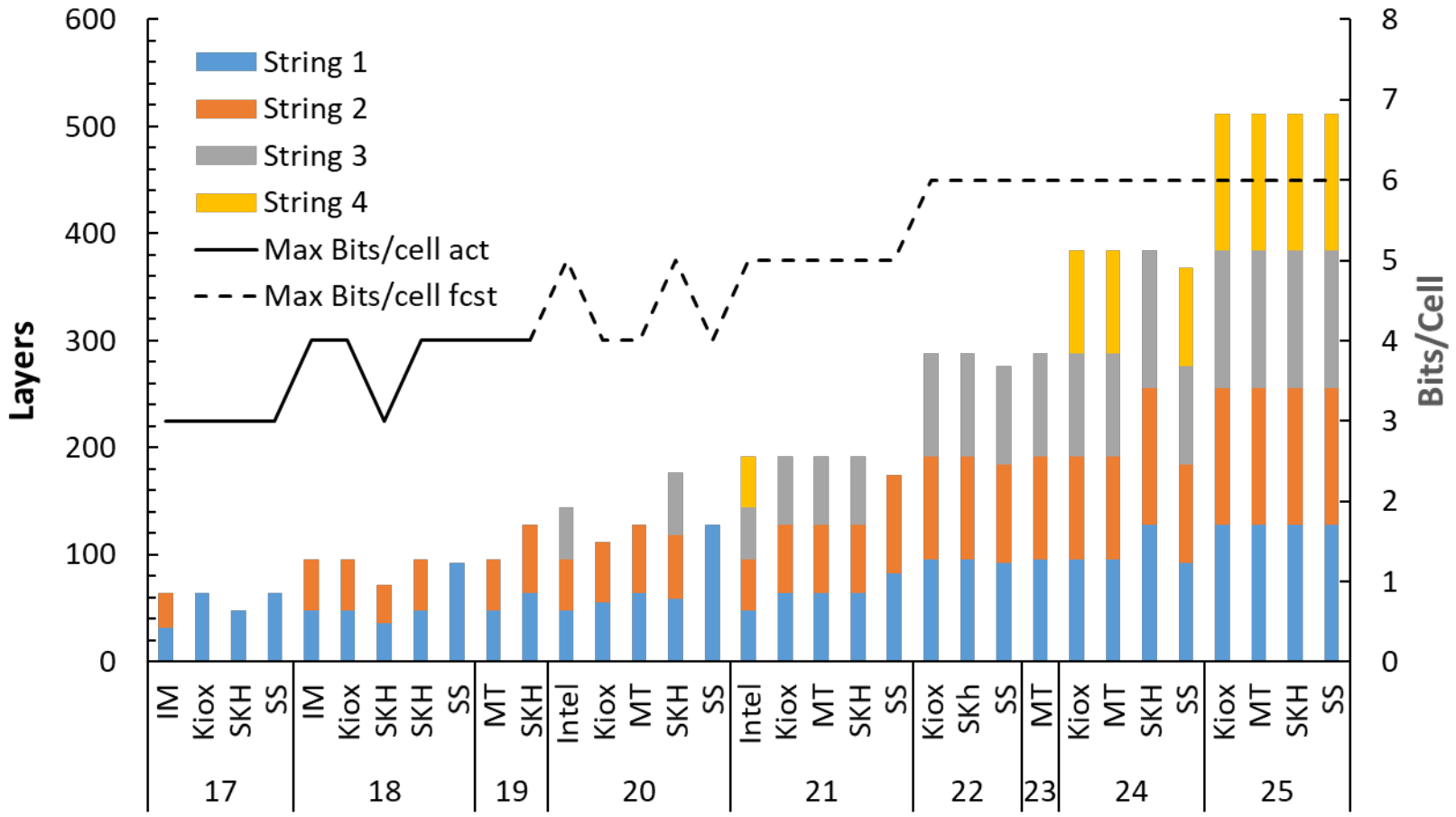


- Deposit alternating layers of SiO and pSi.
- Mask and etch channel hole.
- Recess etch poly, ONO dep, poly dep and etch back.
- Tunnel oxide dep and fill with pSi/SiO
- Deposit SiN, SiO and AlO etch stop layers.
- Mask and etch, fill with pSi.
- Deposit alternating layers of SiO and pSi.
- Mask and etch channel hole.
- Recess etch poly, ONO dep, poly dep and etch back.
- Tunnel oxide dep and fill with pSi/SiO

String stacking (Intel-Micron)

Layers, Stacking and Bits/Cell

- The plot at the right illustrates the number of layers and strings to achieve those layers by year and company.
- The bits/cell is the maximum bits/cell for each year and company.
- SKH has discussed 500 layers in 2025 and 800 layers in 2030.



String Stacking and Bits/cell Versus Year and Company [1]

[1] Strategic Cost Model – 2020 – revision 00

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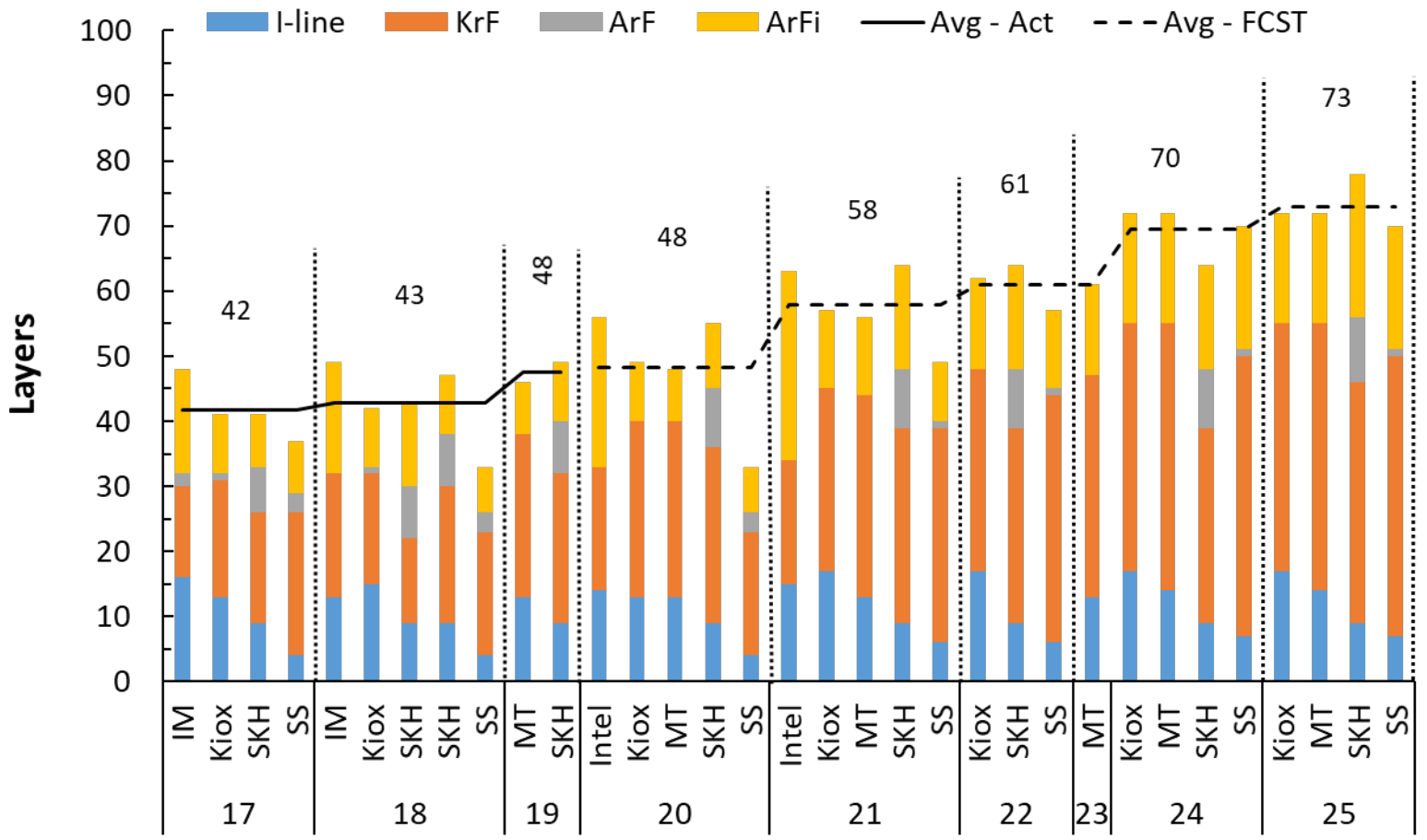
Mask Count Trend

- Mask count trend by year and company.
- We do not expect EUV to be adopted for 3D NAND.



NAND Mask Counts Versus 3D Layers and Company [1]

[1] Strategic Cost Model – 2020 – revision 00

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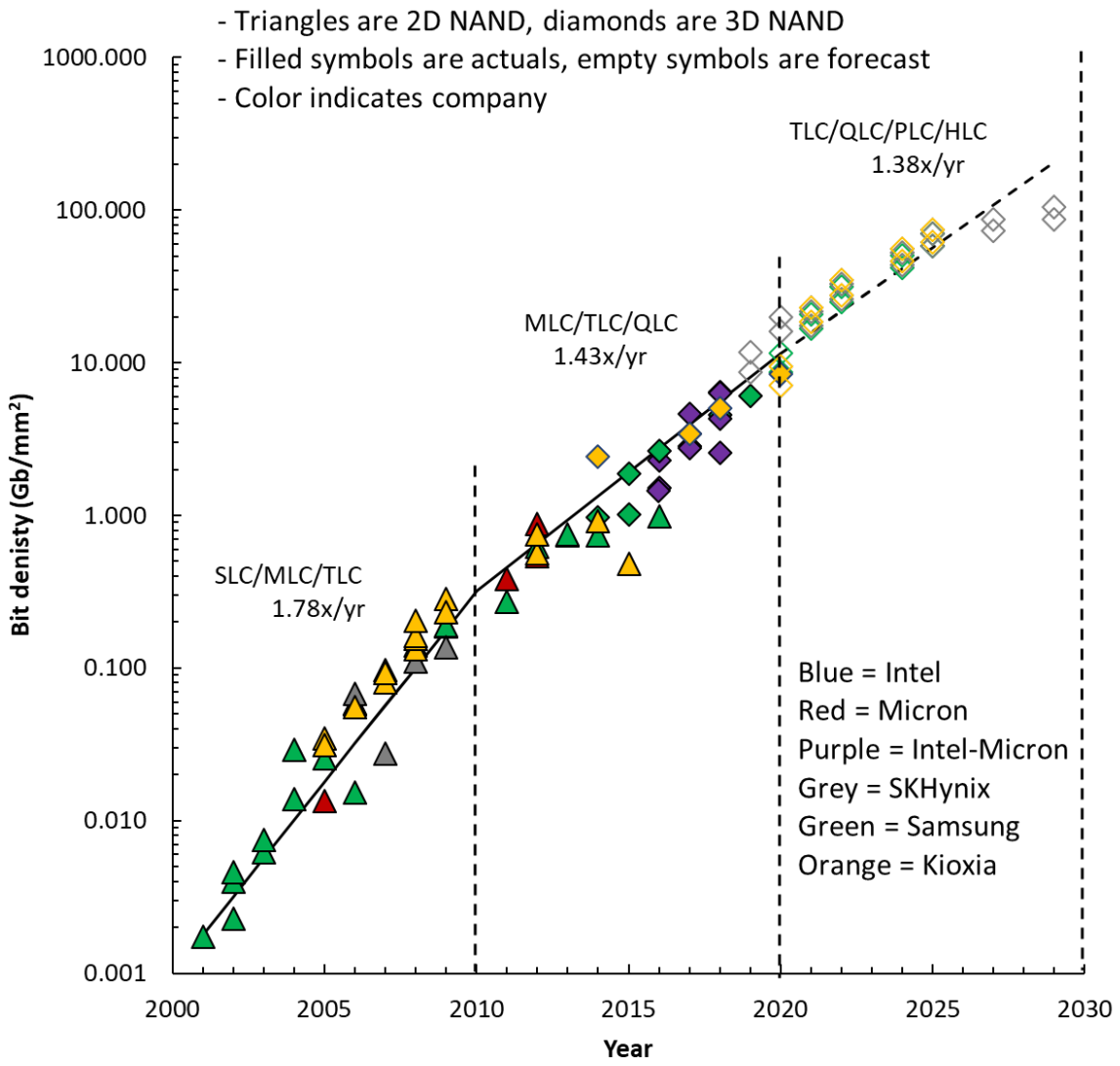
NAND Bit Density

- The transition from 2D NAND to 3D is enabling the continuation in bit density scaling by using the third dimension.
- Bit density is the number of gigabits of memory on the die divided by the die size.
- Multiple points for the same company in the same year represent MLC/TLC/QLC/PLC/HLC.



NAND Bit Density Versus Company and Year [1]

[1] Strategic Cost Model – 2020 – revision 00

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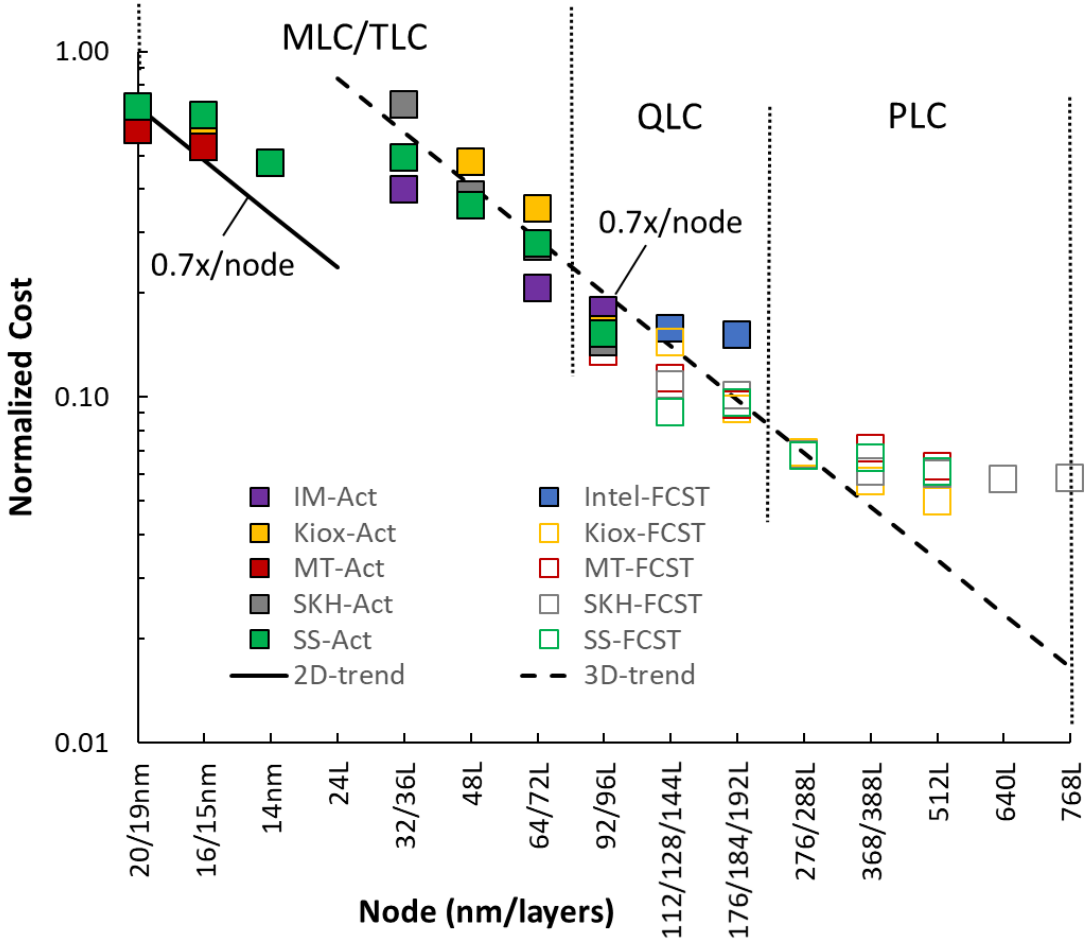
NAND Bit Cost Trend

- Calculated cost per Gb.
- New greenfield fabs in all cases with 75k wpm capacity (current average size for 3D NAND fabs).
- Assumed countries are Singapore for Intel-Micron and Micron, China for Intel, South Korea for Samsung and SK Hynix and Japan for Kioxia.
- Bit density per slide 7.
- Bit cost without taking into account street width or test and packaging costs. Rough die yield approximations used.

[1] Strategic Cost Model – 2020 – revision 00



NAND bit cost trends [1]

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Logic Roadmap

Self consistent node name series

28	20	14	10	7	5	3.5	2.5	1.75
	0.71	0.70	0.71	0.70	0.71	0.70	0.71	0.70

Company nodes and device types by year with transistor density

Company	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Intel	14 (FF) **54.22**					10 (FF) 106.10		7 (FF) 208.05		5 (HNS/FS) **405.17**		3.5 (CFET) **501.26**
Samsung	14 (FF) 34.68		10 (FF) 54.55		7 (FF) 100.59	5 (FF) 133.56	**3.5 (HNS)** **202.85**		**2.5** **(HNS/FS)** **345.95**		**1.75** **(CFET)** **428.00**	
TSMC		16 (FF) 36.06	10 (FF) **55.10**	7 (FF) **101.85**		5 (FF) **185.46**		3.5 (FF) **266.31**		2.5 (HNS/FS) 374.00		1.75 (CFET) 462.70

FF = FinFET, HNS = Horizontal Nanosheet, HNS/FS = Forksheet
HNS, CFET = Complimentary FET with 2 decks

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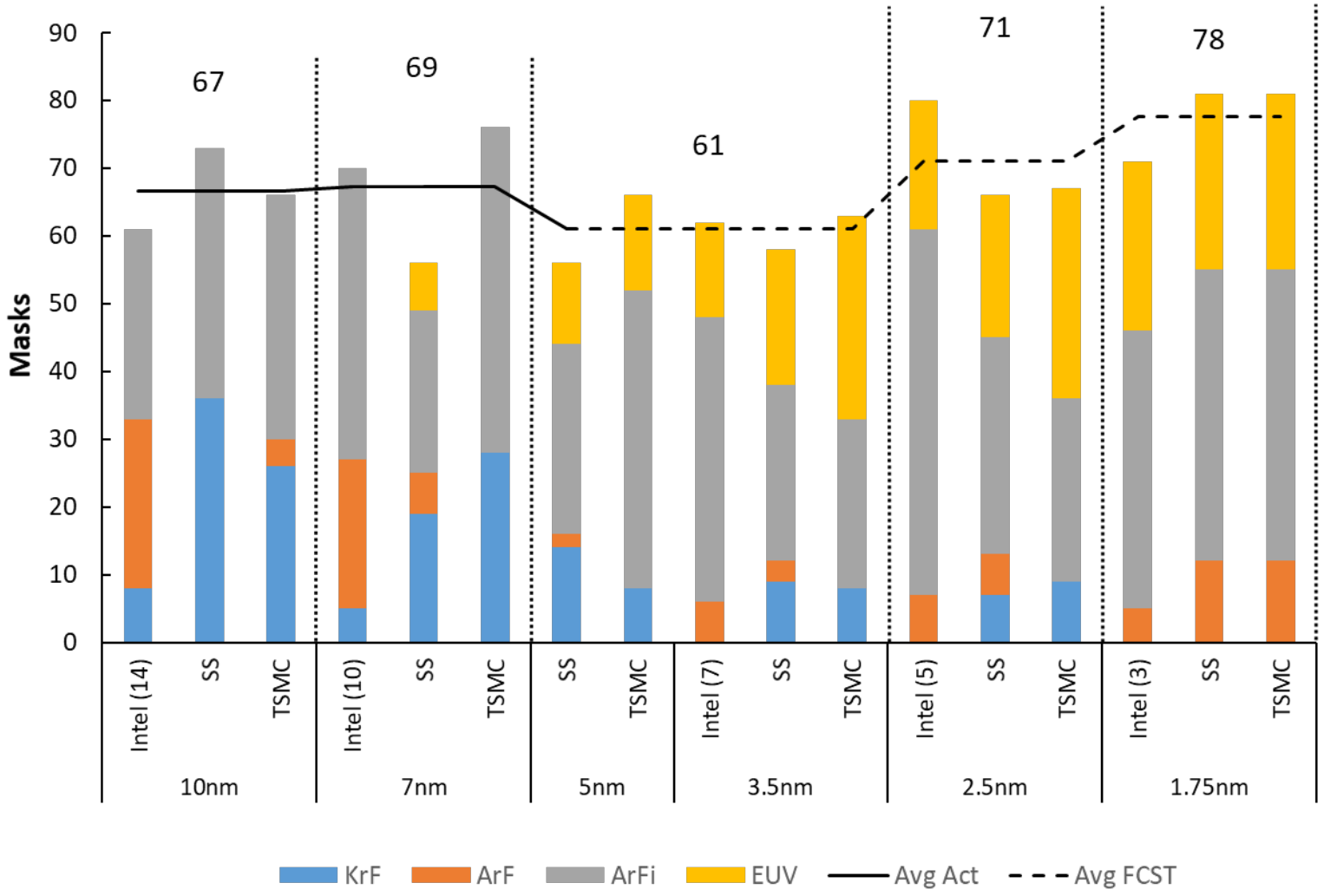
Logic Mask Counts

- Leading edge logic mask count trends by node and company.
- Increasing metal layers and process complexity is driving up mask counts.
- Multi-patterning conversions to EUV reduces mask counts.
- CFET is highly self-aligned reducing the number of EUV layers.

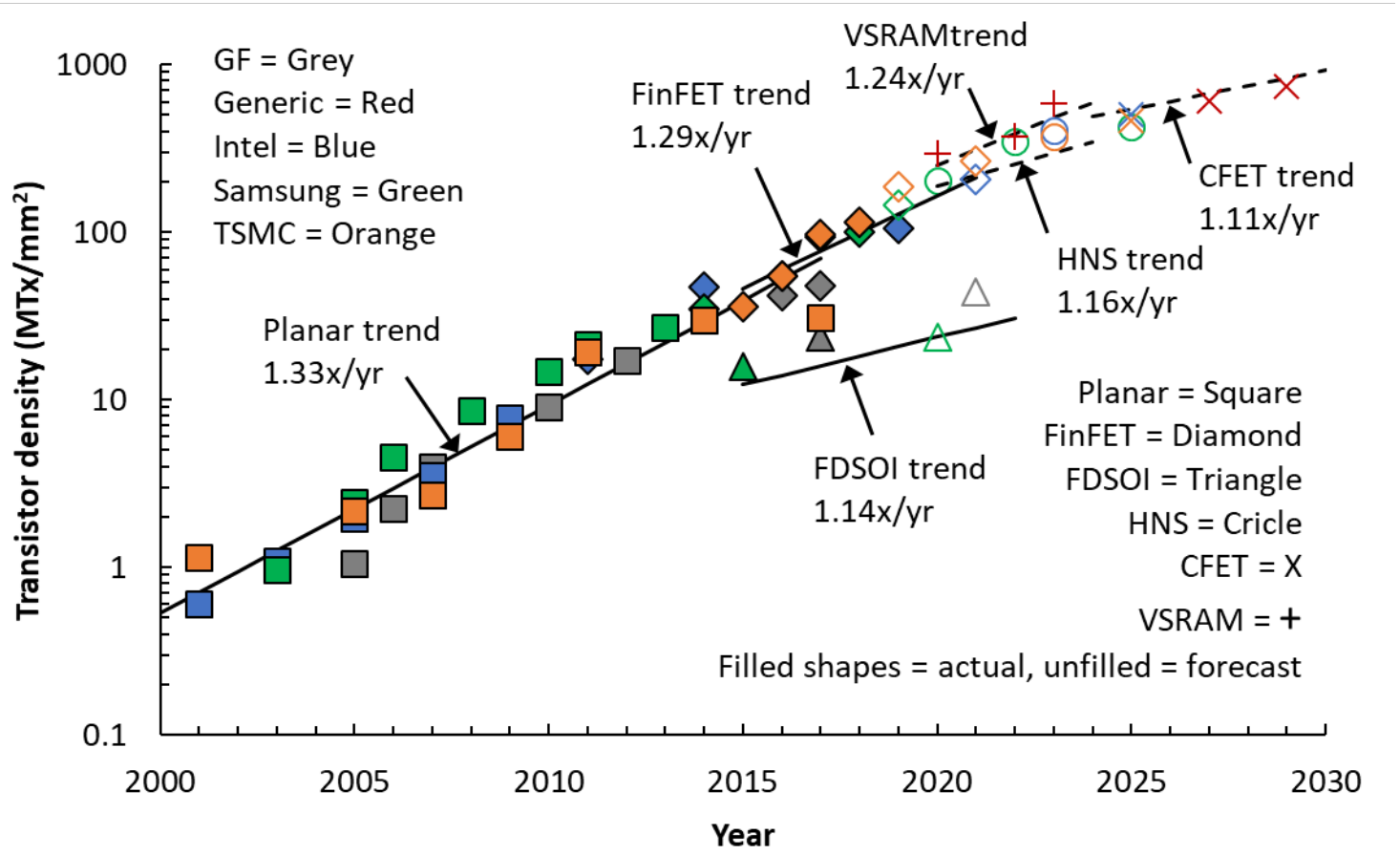


Logic Mask Counts [1]

[1] Strategic Cost Model – 2020 – revision 00

Logic Density Trend

- Transistor density for all processes other than VSRAM is based on the Intel density metric.
- VSRAM is based on projected 6T SRAM cell sizes and 6 transistors per cell.



Logic transistor density trends by company, technology and year [1]

[1] IC Knowledge – Strategic Cost Mode 2020 – revision 00

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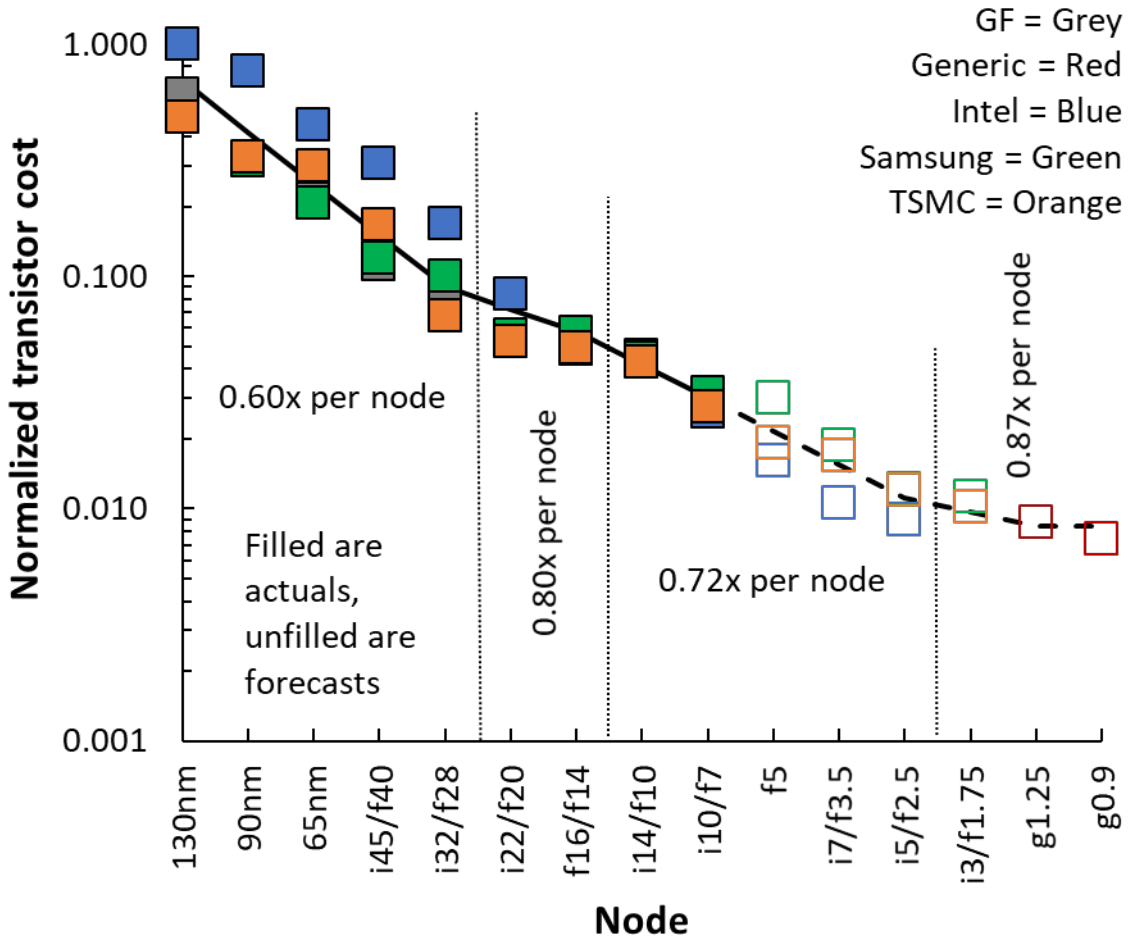
Logic Transistor Cost

- Calculated cost per one billion transistors.
- New greenfield fabs in all cases with 35k wpm capacity (current average size for logic fabs).
- No mask amortization (see the next slide).
- Assumed countries are Germany/US (14nm) for Global Foundries, US/Israel (10nm) for Intel, South Korea for Samsung and Taiwan for TSMC and GNRC.
- Based on transistor density without accounting for yield, street width or edge exclusion.
- Does not consider design costs that are limiting the number of designs that can be run on advanced processes.

[1] IC Knowledge – Strategic Cost Model – 2020 – revision 00



Logic transistor cost trends by company and year [1]

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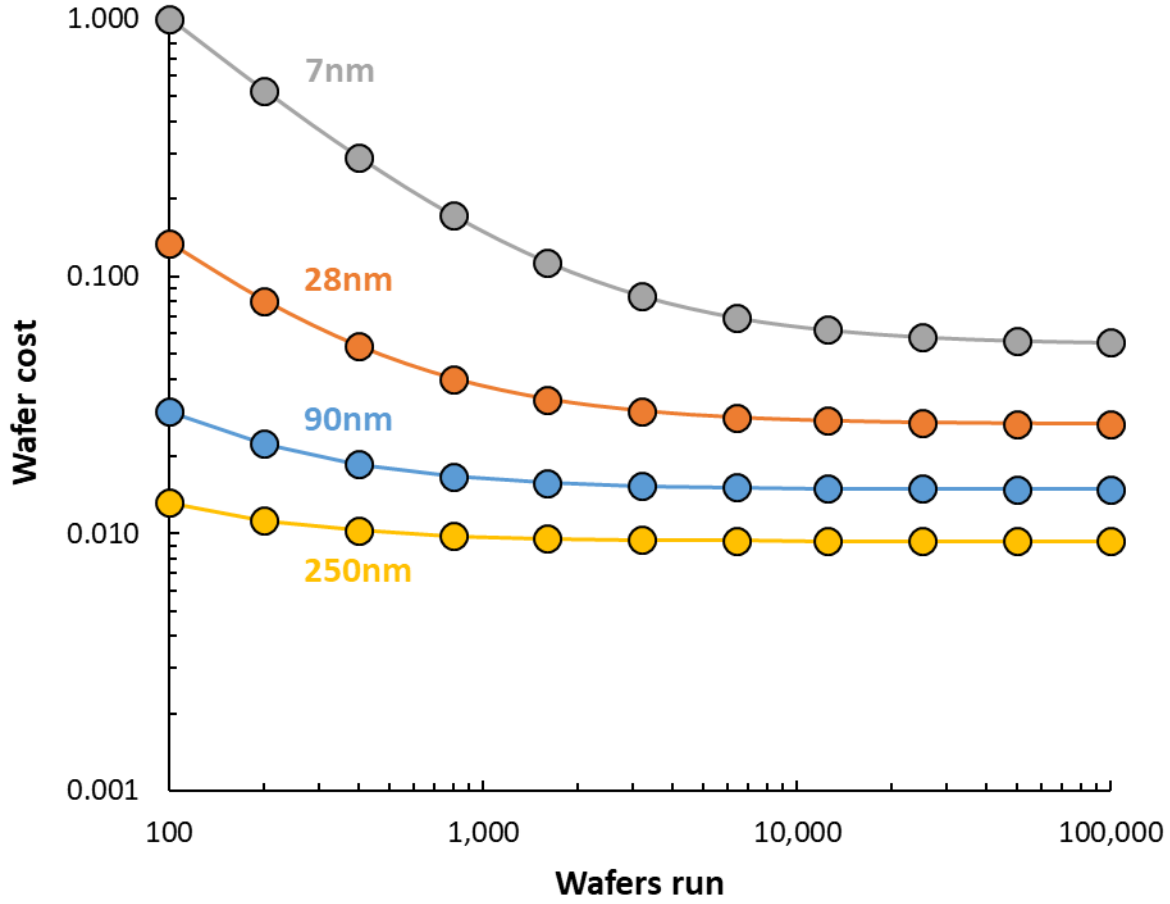
Mask Set Amortization

- Wafer cost with mask set amortization versus node and wafers run per mask set.
- Does not include design cost amortization.
- 40,000 wpm greenfield fab in Taiwan running TSMC processes.

Node	Wafer cost ratio [1]	Mask set cost [2]
250nm	1.42	$43K
90nm	2.00	$165K
28nm	5.04	$1.2M
7nm	18.05	$10.5M

[1] Wafer cost for 100 wafs/mask set divide wafer cost for 100,000 wafs/mask set.
[2] IC Knowledge – Strategic Cost Model – 2020 – revision 00



Logic wafer cost versus node and exposures per mask set [2]

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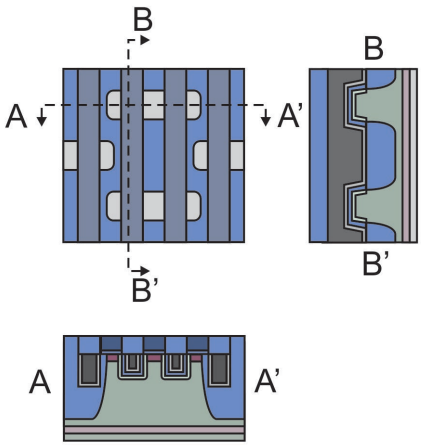
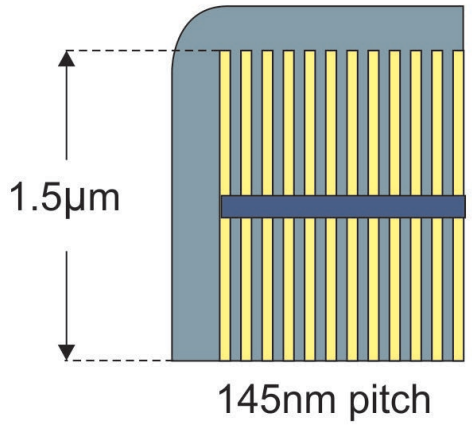
DRAM Nodes

	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Micron Technology		19-1x	16-1y	14-1z		13-1a	12-1b		11-1c	
Samsung	18.5-1x		16-1y	14-1z		13-1a		12-1b		11-1c
SK Hynix			17-1x	16-1y	15 -1z		13-1a	12-1b		11-1c

DRAM nodes are defined as the active half pitch.

Saddle fin <4xnm

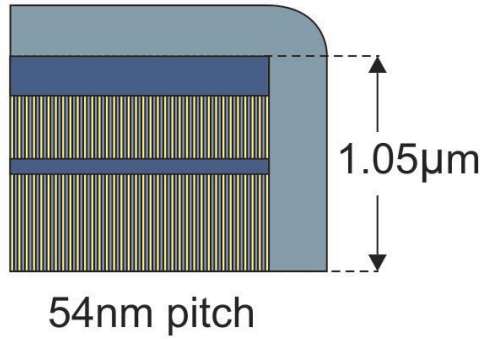




48nm single MESH Capacitor [1]

30% height - 63% pitch

18nm double MESH Capacitor [1]



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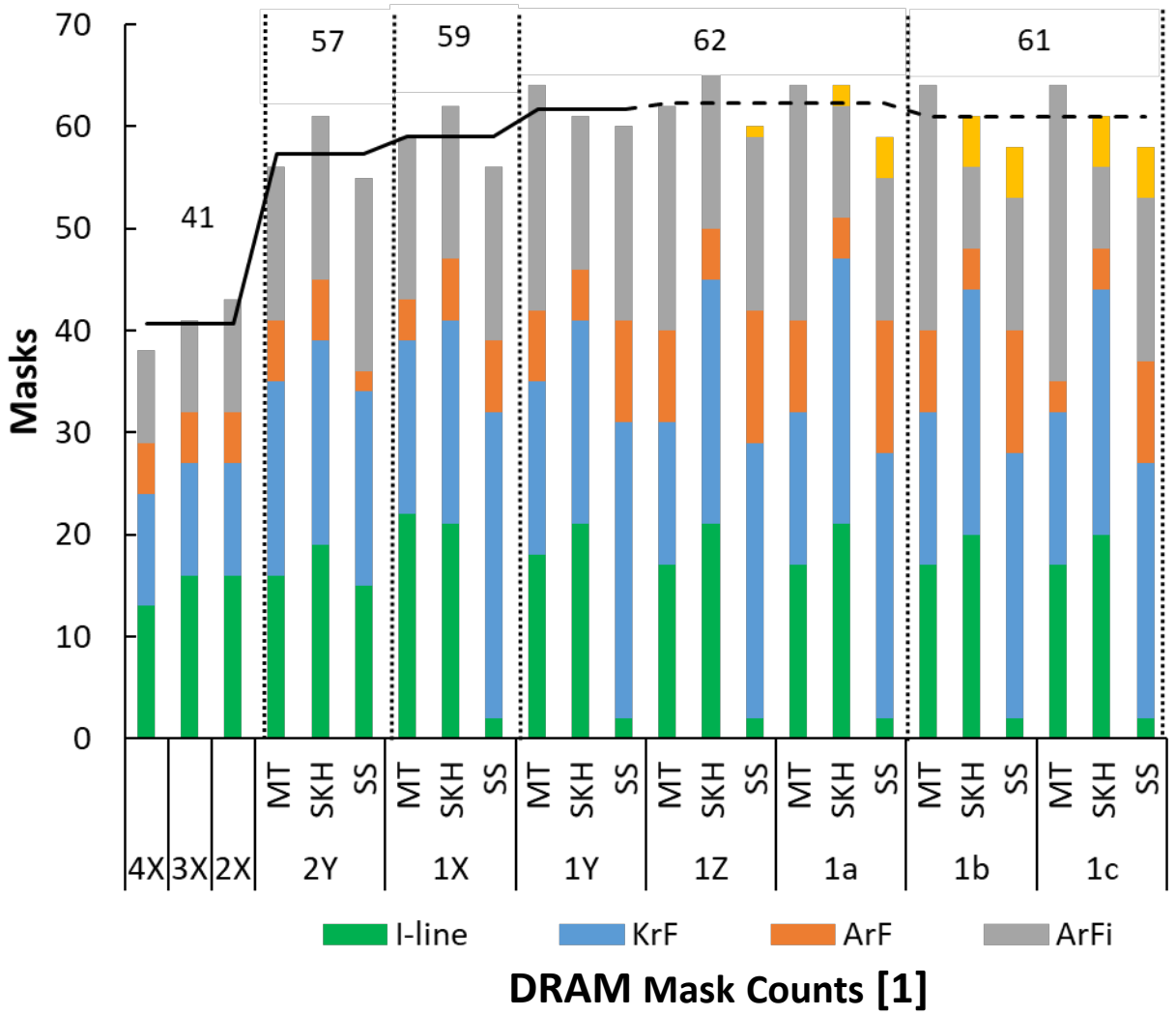
DRAM Mask Counts

- DRAM mask counts by node and company.
- There has been a large increase in mask counts beginning at 2Y.
- Mask counts have increased due to more multi-patterning and more core/peripheral transistor types/thresholds.
- First EUV use at 1z with increased use expected at 1a, 1b, 1c



DRAM Mask Counts [1]

[1] Strategic Cost Model – 2020 – revision 00

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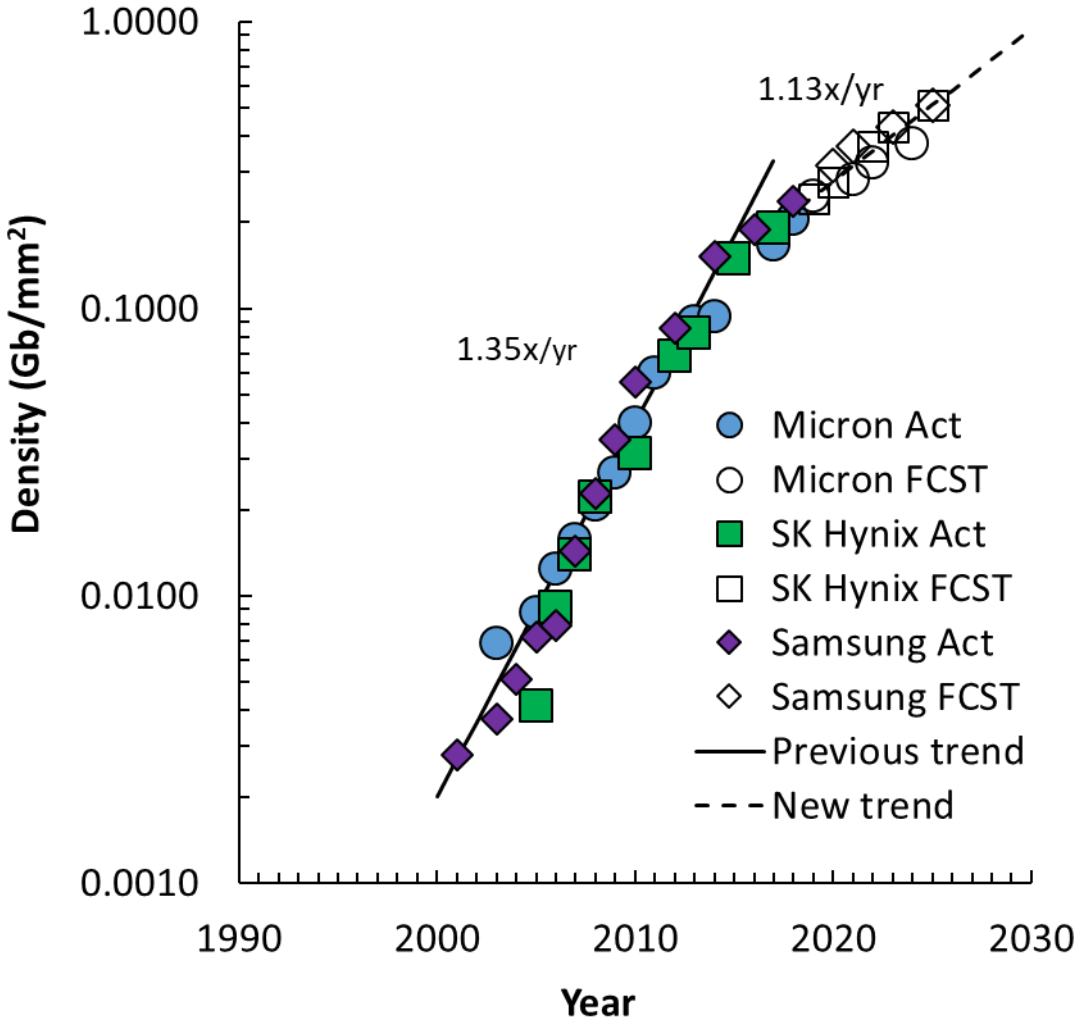
DRAM Bit Density

- Bit density is die capacity in Gb divided by die size in mm^2.
- The solid black line is the long term trend based on actual values.
- The dashed black line is the forecasted trend going forward.



DRAM Bit Density [1]

[1] Strategic Cost Model – 2020 – revision 00

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DRAM Bit Cost

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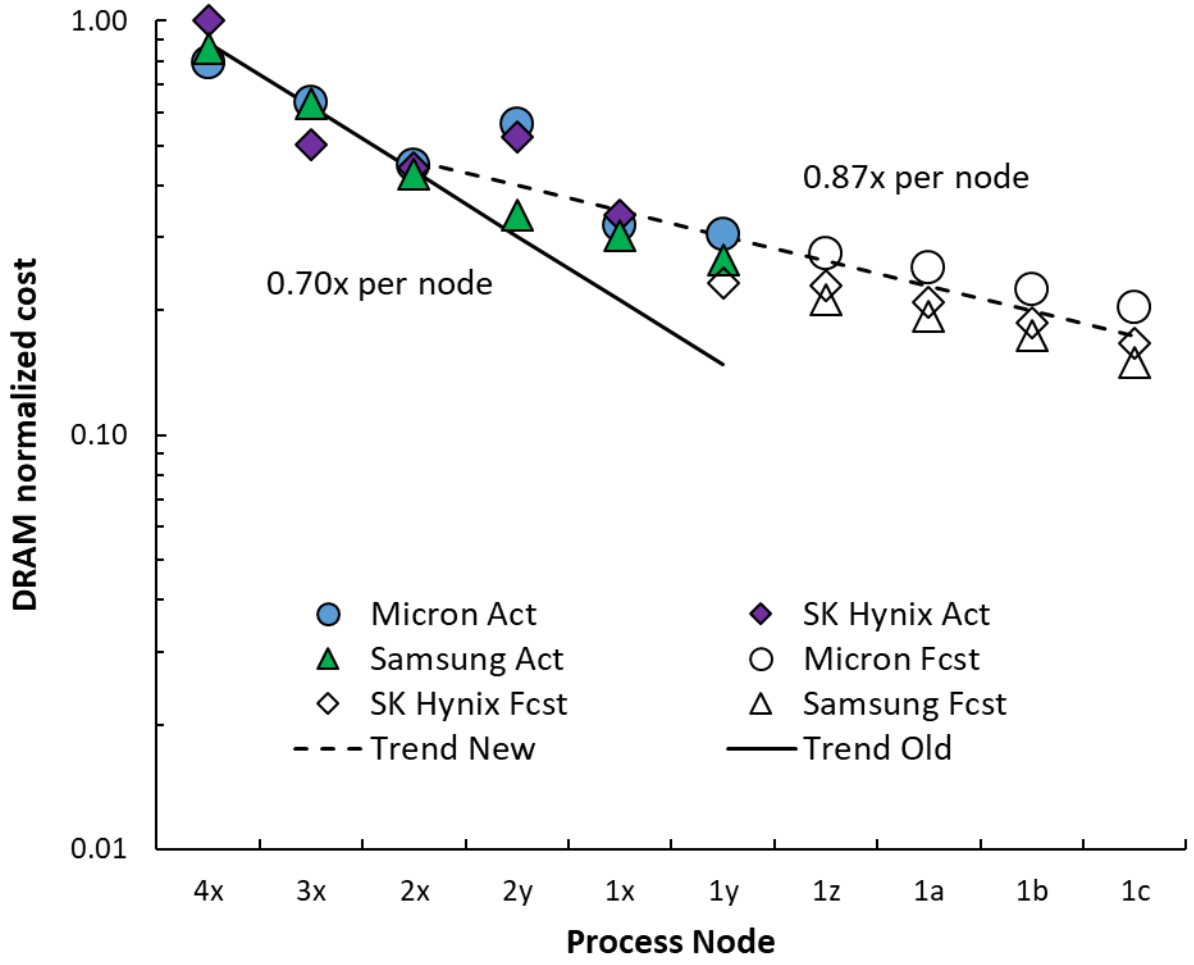
- New greenfield fabs in all cases with 75k wpm capacity (current average size for DRAM fabs).
- Assumed countries are Japan Micron, and South Korea for Samsung and SK Hynix.
- Bit density per slide 16.
- Bit cost without taking into account street width or test and packaging costs.



DRAM bit cost trends by company and year [1]

[1] IC Knowledge – Strategic Cost Model – 2020 – revision 00

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Conclusion

- 3D NAND
  - Scaling path to the mid to late 2020s
  - Bit cost may not scale beyond 400 layers
- Logic
  - Scaling path to the end of the 2020s with CFETs
  - Mask and design costs will limit the number of products that can take advantage of the latest technologies
- DRAM
  - Scaling and bit cost reductions have slowed
  - No clear answer to address scaling