TSMC 2019 Open Innovation Platform® Theater, Booth #326

	Monday 6/3		Tuesday 6/4		Wednesday 6/5	
10:15am	**Analog Bits**	Low Power Analog Foundation IP in 7nm and 5nm	**M31**	Enable your AI and IOT with M31 Silicon IP	**Silicon Creations**	Comparing silicon to simulations for a 1.3pJ/bit 25Gbps SerDes Rx in TSMC 28HPC+
10:30am	**Mentor**	Partnering to Address Mutual Customers Requirements in nm Technologies	**Cadence**	High-Speed Interface IP for Advanced Process Nodes	**Rambus**	Advanced Memory Interfaces for High-Performance Systems
10:45am	**IMEC**	Automotive Radar, AR and IOT: A Snapshot Of imec Technology in TSMC's Process	**Dorado**	Advanced ECO Solution in FinFET Technology Nodes	**Microchip**	
11:00am			**Raffle / Break**			
11:15am	**Moortec**	In-Chip Monitoring Trends for AI & Data Center Applications	**ANSYS**	ANSYS Multiphysics Enable Silicon Success	**Arm**	Arm automotive physical IP addresses new feature and functionality demands
11:30am	**True Circuits**	True Collaboration – DDR 4/3 PHY	**Microsoft**	Azure for Silicon Design	**Silvaco**	From Atoms to Systems
11:45am	**Amazon**	Cloud-Based Innovation for Semiconductor Design and Manufacturing	**Mentor**	Key considerations for IC/MEMS co-design	**eMemory**	Robust Logic NVM and Security Solutions
12:00pm			**Raffle / Break**			
1:30pm	**Arm**	Implementing Cloud to the Edge Infrastructure with Neoverse POP IP	**Rambus**	dvanced Memory Interfaces for High-Performance Systems	**SiFive**	The World's First Chip Designed Entirely in the Cloud
1:45pm	**M31**	Enable your AI and IOT with M31 Silicon IP	**Arm**	Build Energy-Efficient SoCs Using Artisan Physical IP on TSMC 22nm	**Synopsys**	Synopsys Custom Platform Enablement for TSMC
2:00pm	**ANSYS**	ANSYS Multiphysics Enable Silicon Success	**Amazon**	Cloud-Based Innovation for Semiconductor Design and Manufacturing	**Moortec**	In-Chip Monitoring Trends for AI & Data Center Applications
2:15pm	**eMemory**	Robust Logic NVM and Security Solutions	**IMEC**	Automotive Radar, AR and IOT: A Snapshot Of imec Technology in TSMC's Process	**Microsoft**	Azure for Silicon Design
2:30pm			**Raffle / Break**			
2:45pm	**Silicon Creations**	Comparing silicon to simulations for a 1.3pJ/bit 25Gbps SerDes Rx in TSMC 28HPC+	**SiFive**	The World's First Chip Designed Entirely in the Cloud	**Mentor**	Test for AI, next level of quality and SoC DFT architecture
3:00pm	**Dorado**	Advanced ECO Solution in FinFET Technology Nodes	**Avatar**	2X faster Design Closure times, better QoR, with Avatar Place & Route Solution	**M31**	Enable your AI and IOT with M31 Silicon IP
3:15pm	**Synopsys**	Silicon-Proven DesignWare IP for TSMC Processes	**Cadence**	Full-Flow Digital Solution for 5nm SoC Design	**IMEC**	Automotive Radar, AR and IOT: A Snapshot Of imec Technology in TSMC's Process
3:30pm	**Mentor**	Chip Verification in Today's Market is Advanced DRC and so Much More!	**eMemory**	Robust Logic NVM and Security Solutions	**Dorado**	Advanced ECO Solution in FinFET Technology Nodes
3:45pm	**Cadence**	The Cadence Cloud Portfolio	**Silvaco**	From Atoms to Systems	**Amazon**	Cloud-Based Innovation for Semiconductor Design and Manufacturing
4:00pm			**Raffle / Break**			
4:15pm	**SiFive**	The World's First Chip Designed Entirely in the Cloud	**Silicon Creations**	Comparing silicon to simulations for a 1.3pJ/bit 25Gbps SerDes Rx in TSMC 28HPC+	**Analog Bits**	Low Power Analog Foundation IP in 7nm and 5nm
4:30pm	**Rambus**	Advanced Memory Interfaces for High-Performance Systems	**Moortec**	In-Chip Monitoring Trends for AI & Data Center Applications	**Cadence**	Custom, Analog, and Mixed-Signal Design Flows for Advanced Nodes
4:45pm	**Silvaco**	From Atoms to Systems	**Synopsys**	Enabling the Next Wave of Design Innovation for 7nm FinFET and Beyond	**Andes**	Instruction Customization in RISC-V
5:00pm	**Microsoft**	Azure for Silicon Design	**Analog Bits**	Low Power Analog Foundation IP in 7nm and 5nm	**ANSYS**	ANSYS Multiphysics Enable Silicon Success
5:15pm	**TSMC**	TSMC Open Innovation Platform Updates	**TSMC**	TSMC Open Innovation Platform Updates	**TSMC**	TSMC Open Innovation Platform Updates
5:30pm			**Raffle**			