Leading Edge Logic Comparison

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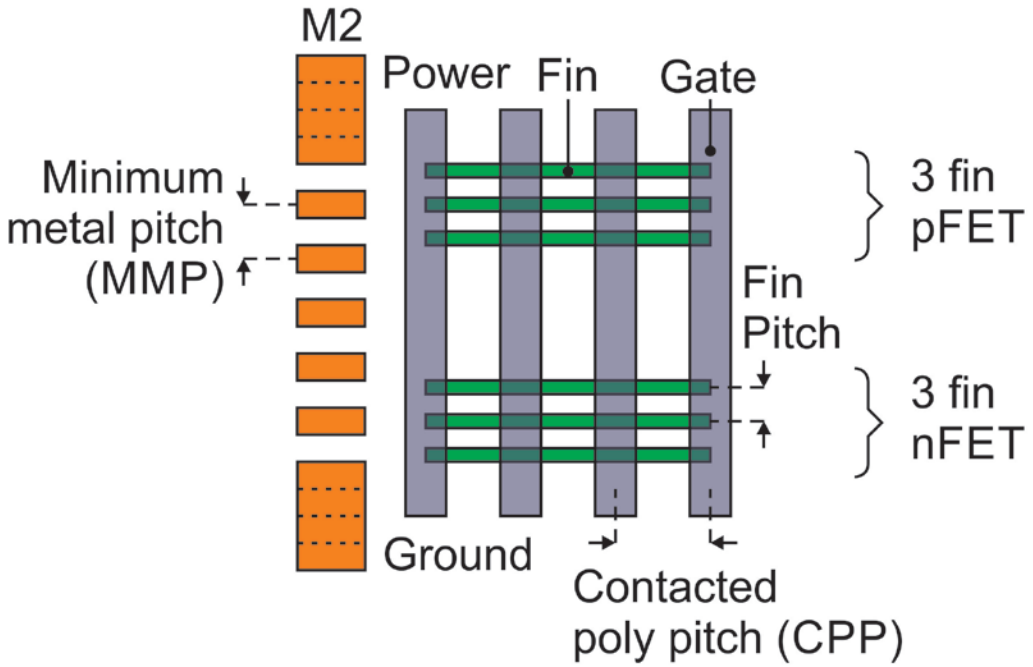
Logic Standard Cell

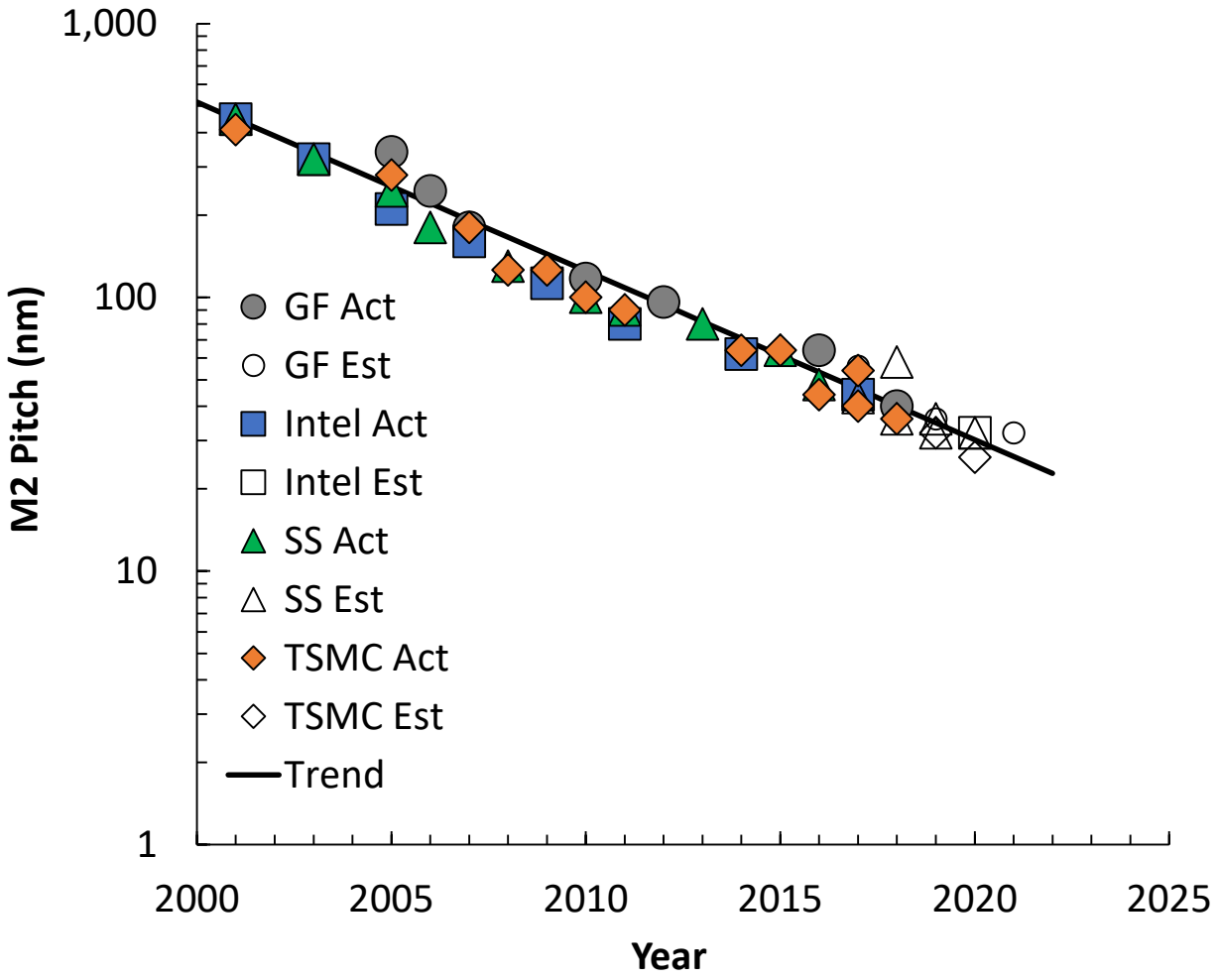
- Logic designs are created using standard cells.
- The cell height is the number of tracks multiplied by the metal pitch.
- Tracks and pitch are measured in metal 2.
- A 7.5 track cell is shown, one half of the power and ground rail heights are in the cell above and cell below respectively.



7.5 track logic cell

Metal 2 Pitch

- The figure on the right presents the metal 2 pitch for the four companies driving the lading edge for logic:
  - GLOBALFOUNDRIES
  - Intel
  - Samsung
  - TSMC
- Solid filled markers are actual values, unfilled markers are IC Knowledge estimates.
- The trend is based on actuals only.



M2 Pitch Trend

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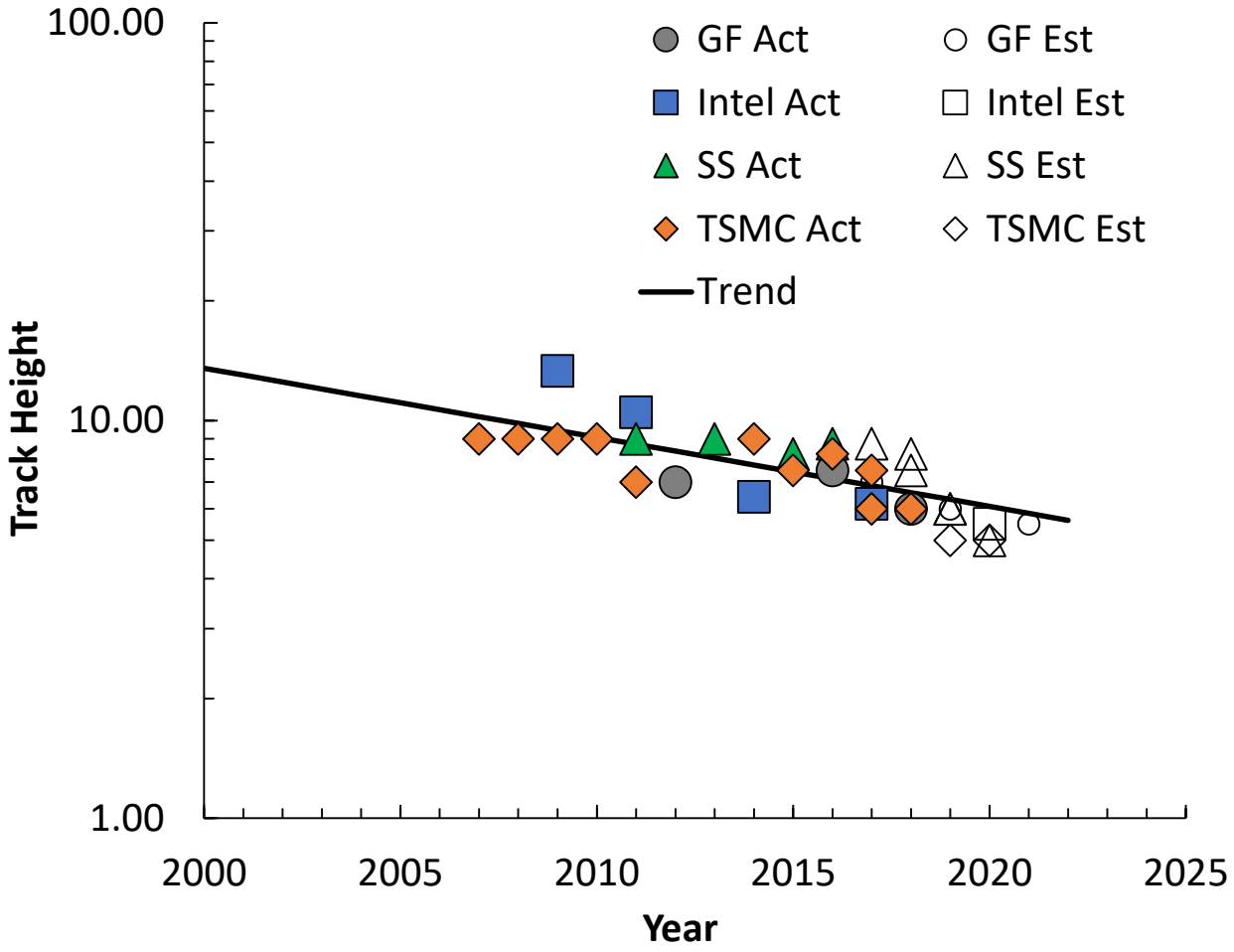
Track Heights

- The figure on the right presents the track heights for the four companies driving the lading edge for logic.
- Solid filled markers are actual values, unfilled markers are IC Knowledge estimates.
- Reducing track height to drive shrinks is becoming more prevalent with recent and projected processes below the trend line.
- The trend is based on actuals only.



Track Heights

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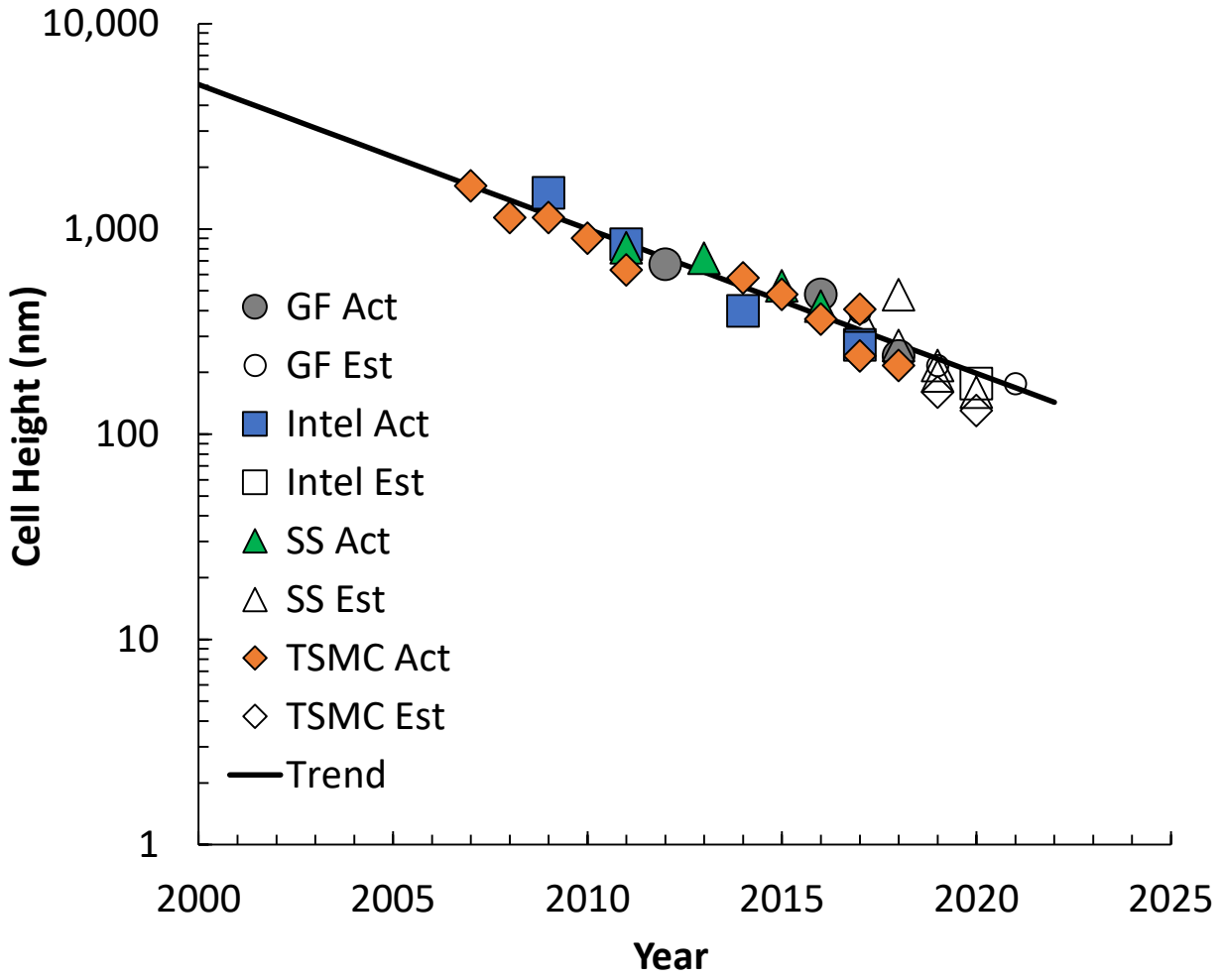
Cell Heights

- Combining the previous two slides we get the figure on the right presenting the cell heights for the four companies driving the leading edge for logic.
- Solid filled markers are actual values, unfilled markers are IC Knowledge estimates.
- The trend is based on actuals only.



Cell Heights

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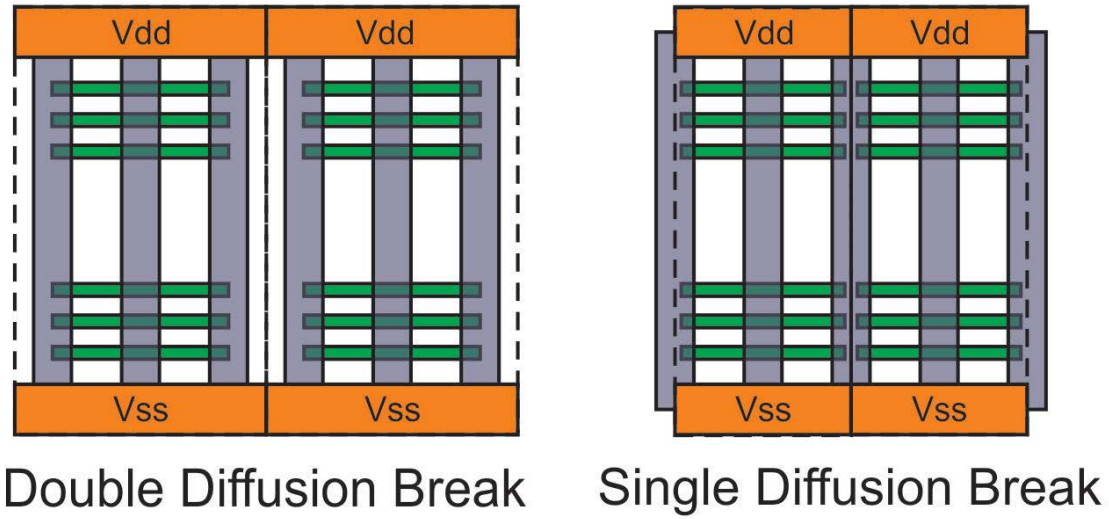
Cell Widths

- The cell width is related to the contact poly pitch (CPP).
- The number of CPPs that make up the cell width depend on the cell type and whether the cell has a double diffusion break (DDB) or single diffusion break (SDB).
- A DDB adds an addition one half CPP to each side of a cell so that in the case illustrated on the right the cells are 3x CPP for the DDB or 2x CPP for the SDB.



Double versus single diffusion break

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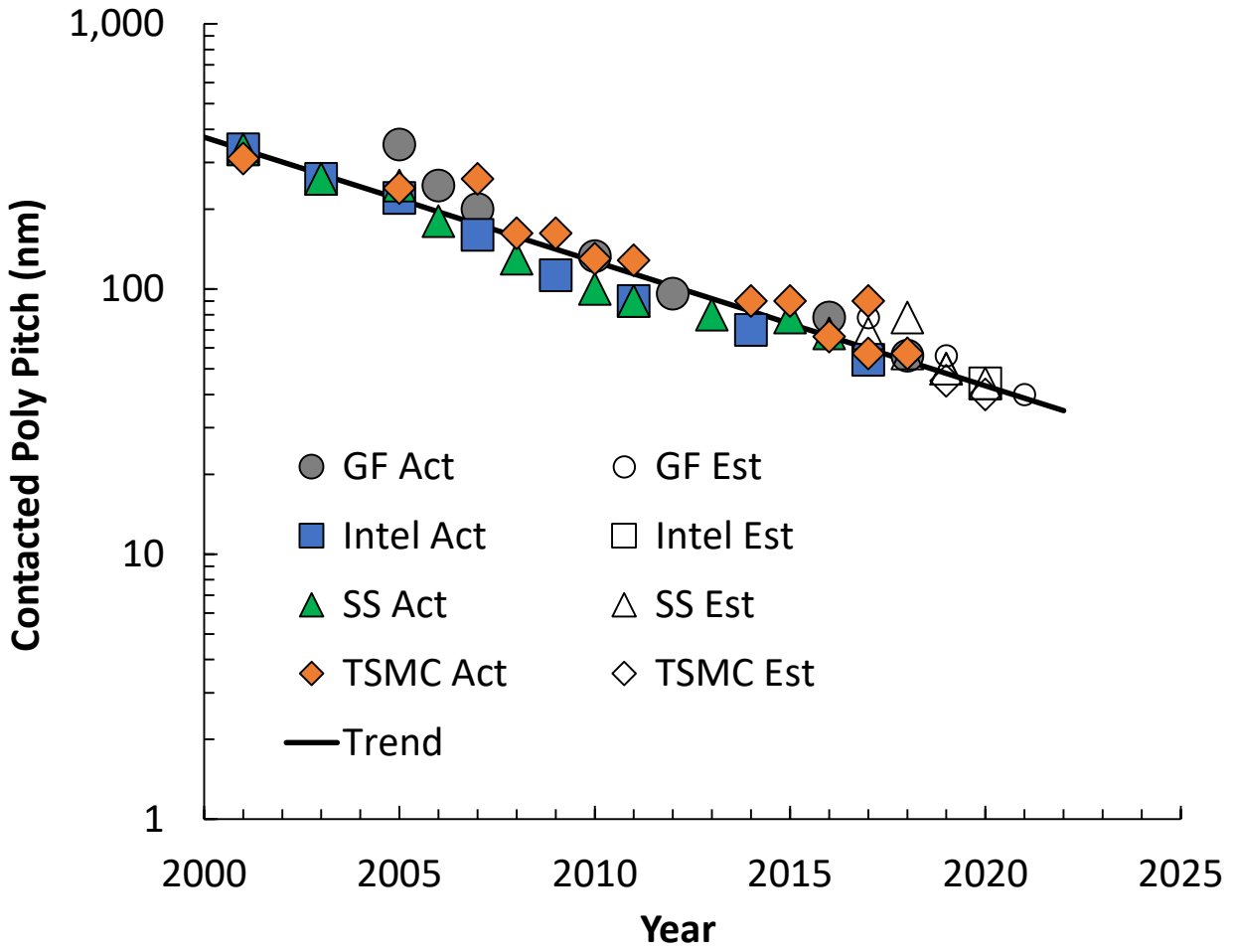
SDB and DDB Usage

- For the four manufacturers:
  - GLOBALFOUNDRIES
  - Intel
  - Samsung
  - TSMC
- There are a variety of SDB and DDB usages depending on node and sometimes process variants within a node.

Contacted Poly Pitch

- The figure on the right presents the contacted poly pitch for the four companies driving the lading edge for logic.
- Solid filled markers are actual values, unfilled markers are IC Knowledge estimates.
- Note that CPP is limited to about 40nm due to device issues.
- The trend is based on actuals only.



Contacted Poly Pitch

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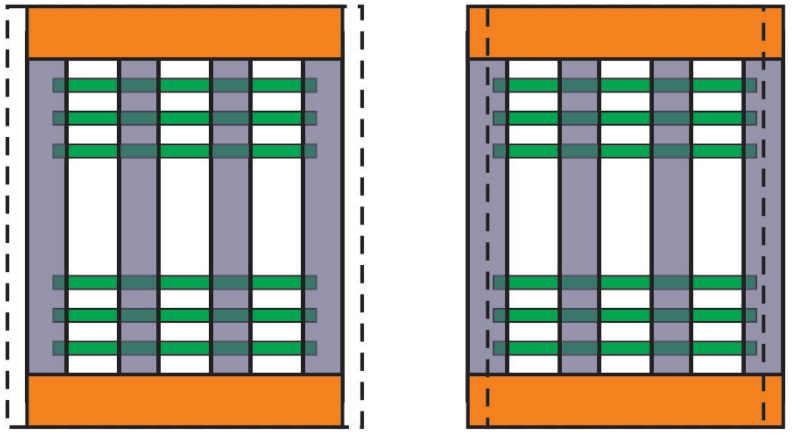
Logic Cells – Two Input NAND Cell

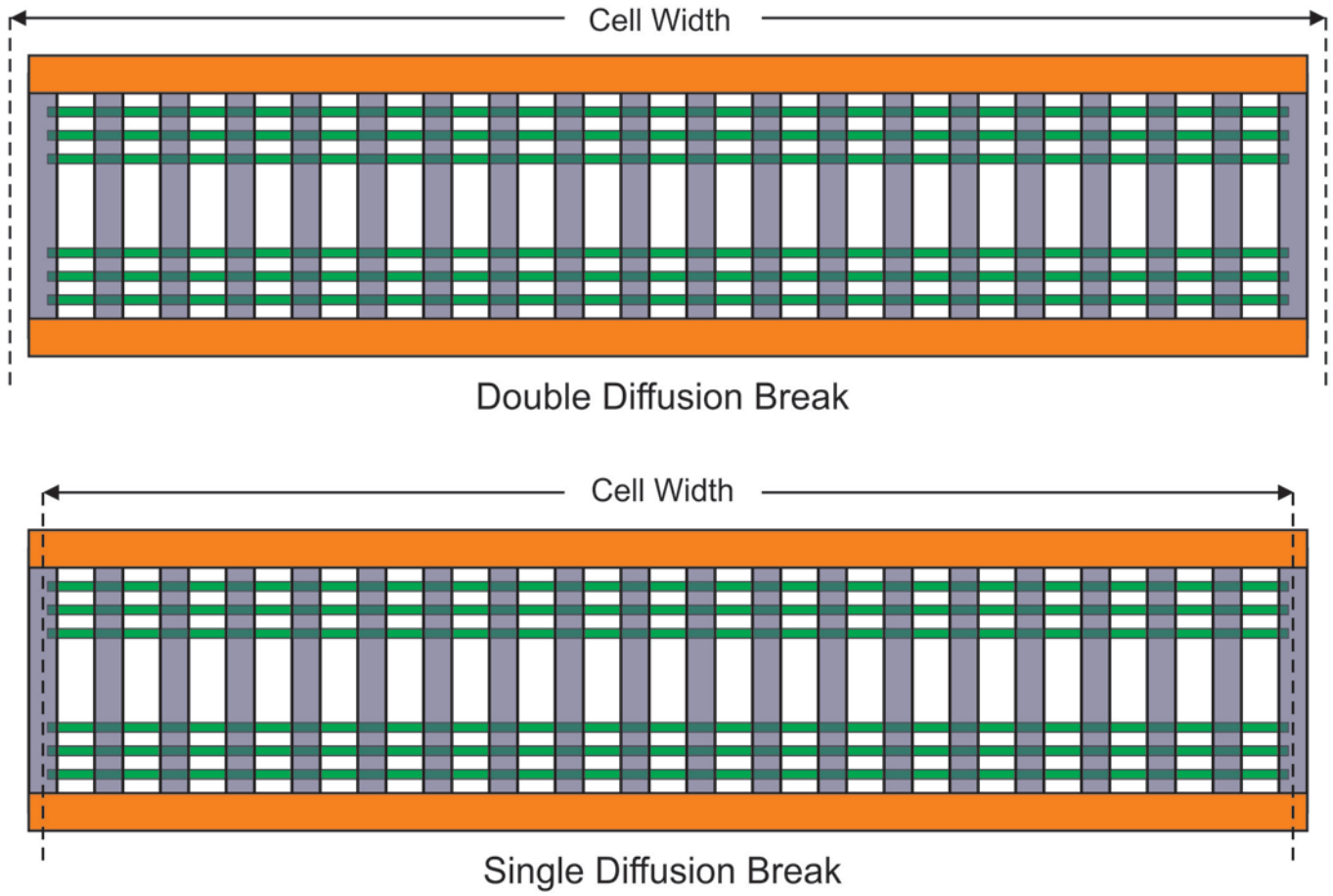
- One of the most common logic cells is the two input NAND gate.
- The figure at the right illustrates DDB and SDB two input NAND cells.
- A DDB - two input NAND cell is 4x CPP wide and a SDB - two input NAND cell is 3x CPP wide.



Double versus single diffusion break
Two input NAND cells

More Logic Cells – Scanned Flip Flop

- Another common logic cell is the Scanned Flip Flop (SFF).
- The figure at the right illustrates DDB and SDB SFF.
- A DDB - SFF cell is 20x CPP wide and a SDB - SFF cell is 19x CPP wide.



Double versus single diffusion break Scanned flip flop

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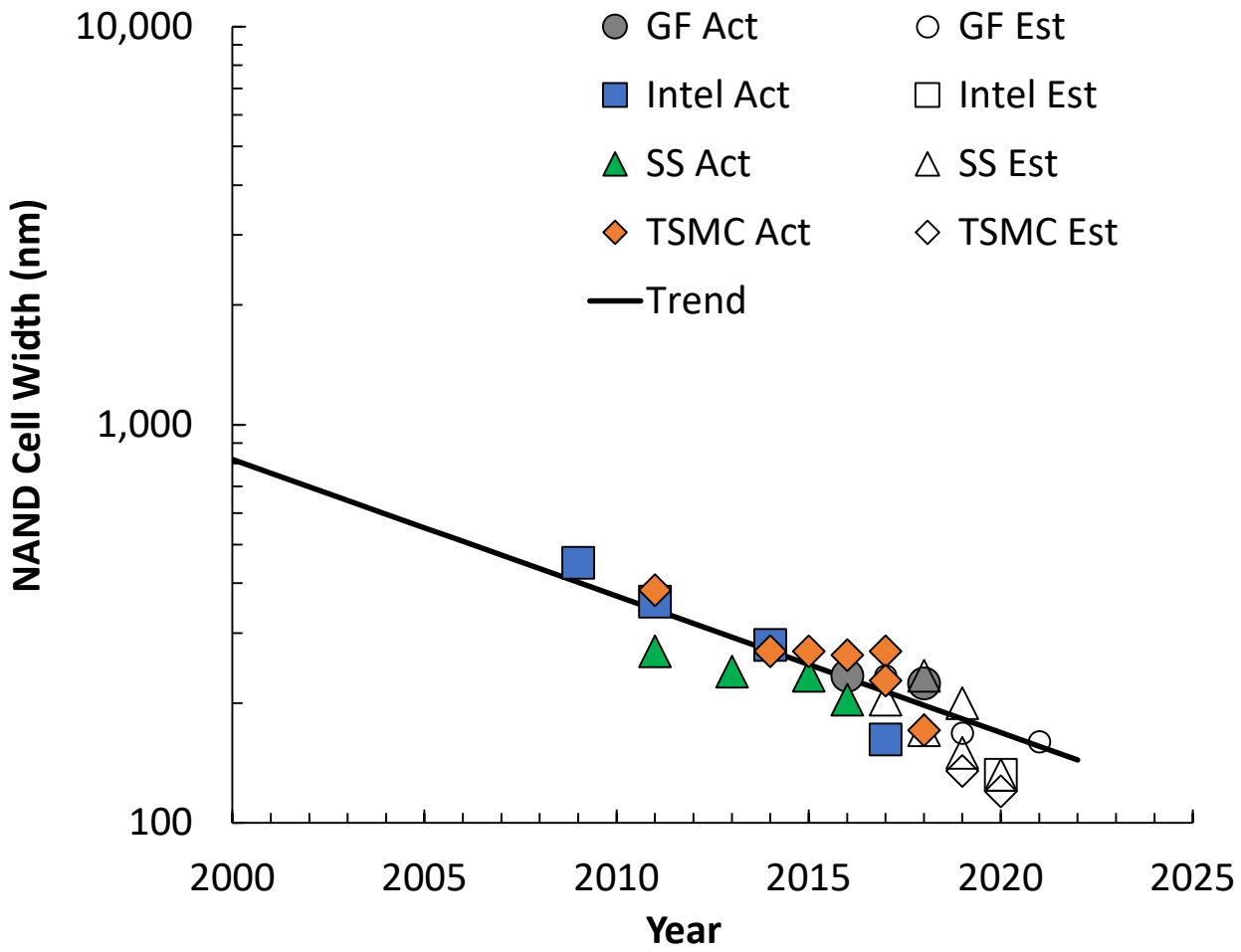
2 Input NAND Cell Width

- Taking into account CPP and DDB versus SDB usage by company cell widths for two input NAND cells can be calculated.
- The plot on the right resents the cell widths for the four companies of interest by year.
- The trend is based on actuals only.



2 Input NAND Cell Width

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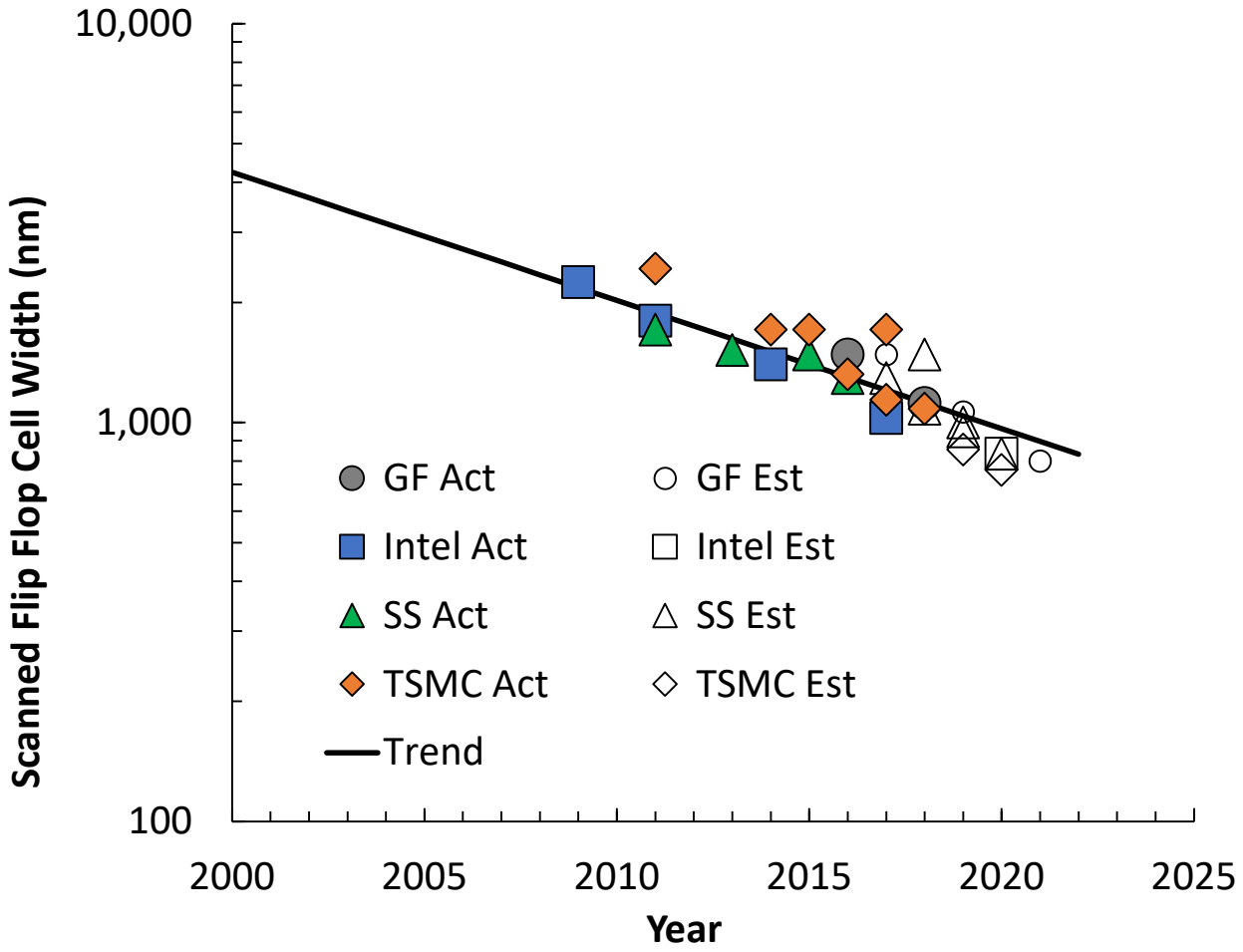
Scanned Flip Flop Cell Width

- Taking into account CPP and DDB versus SDB usage by company cell widths for scanned flip flop cells can be calculated.
- The plot on the right resents the cell widths for the four companies of interest by year.
- The trend is based on actuals only.



Scanned Flip Flop Cell Width

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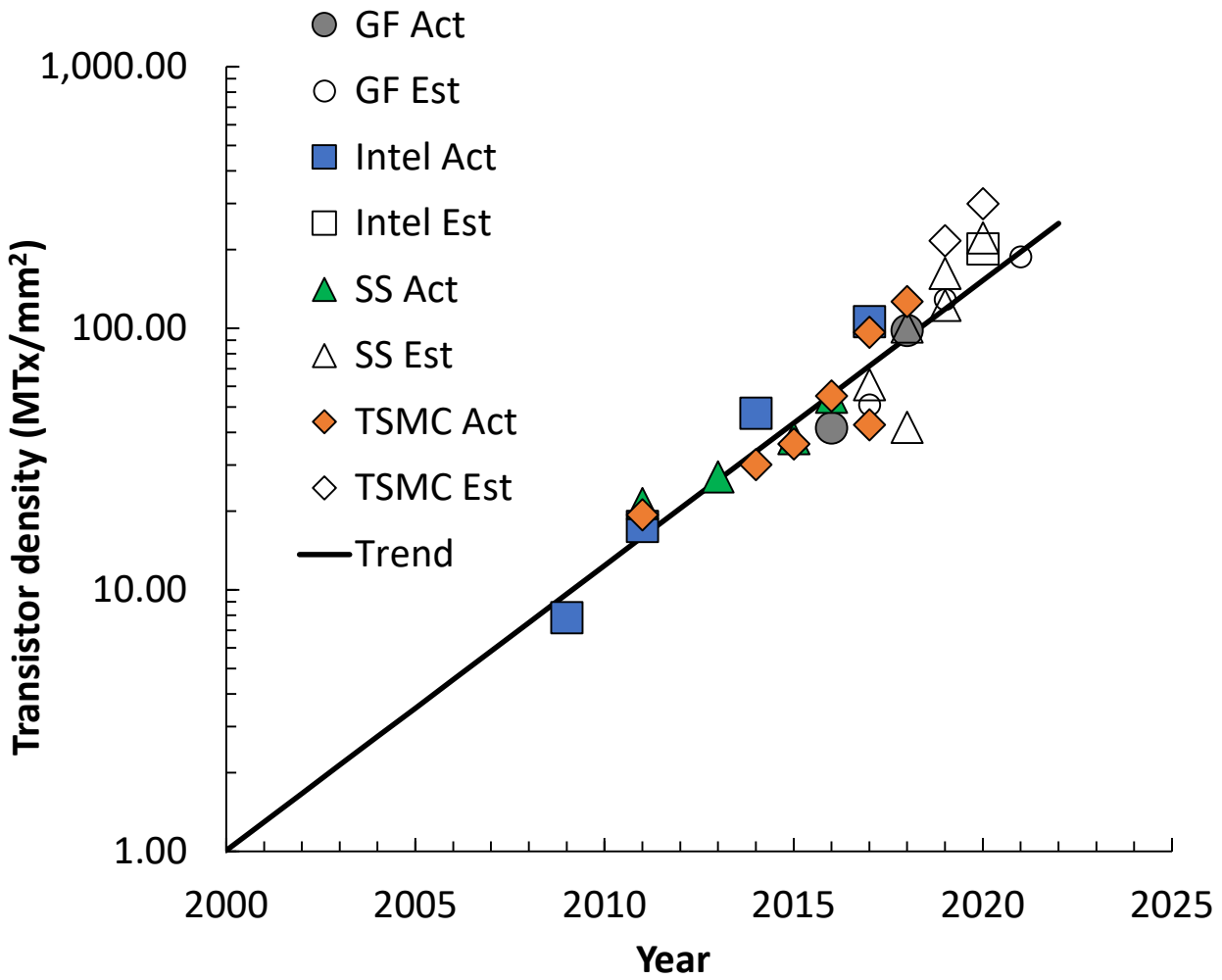
Logic Process Density

- From the previous five slides it can be seen that the width of a logic cell depends on SDB versus DDB and what kind of cell it is.
- Intel has proposed revising an old metric of logic density based on a weighting of 60% two input NAND cells and 40% scanned flip flops. This meant to reflect the rough prevalence of the cell usage in logic designs.
- A cell sizes for two input NAND and scanned flip flops are the cell height and widths outlined previously.
- A two input NAND cell contains 4 transistors and a scanned flip flop cell contains 36 transistors.
- Based on the cells sizes and transistors per cell the cell type weighting can be used to produce transistor densities by process.

Transistor Density

- Using the proposed Intel transistor density metric, process density by year can be compared by year for the four companies of interest.
- The trend line is based on actuals only.



Millions of Transistors Per Square Millimeter

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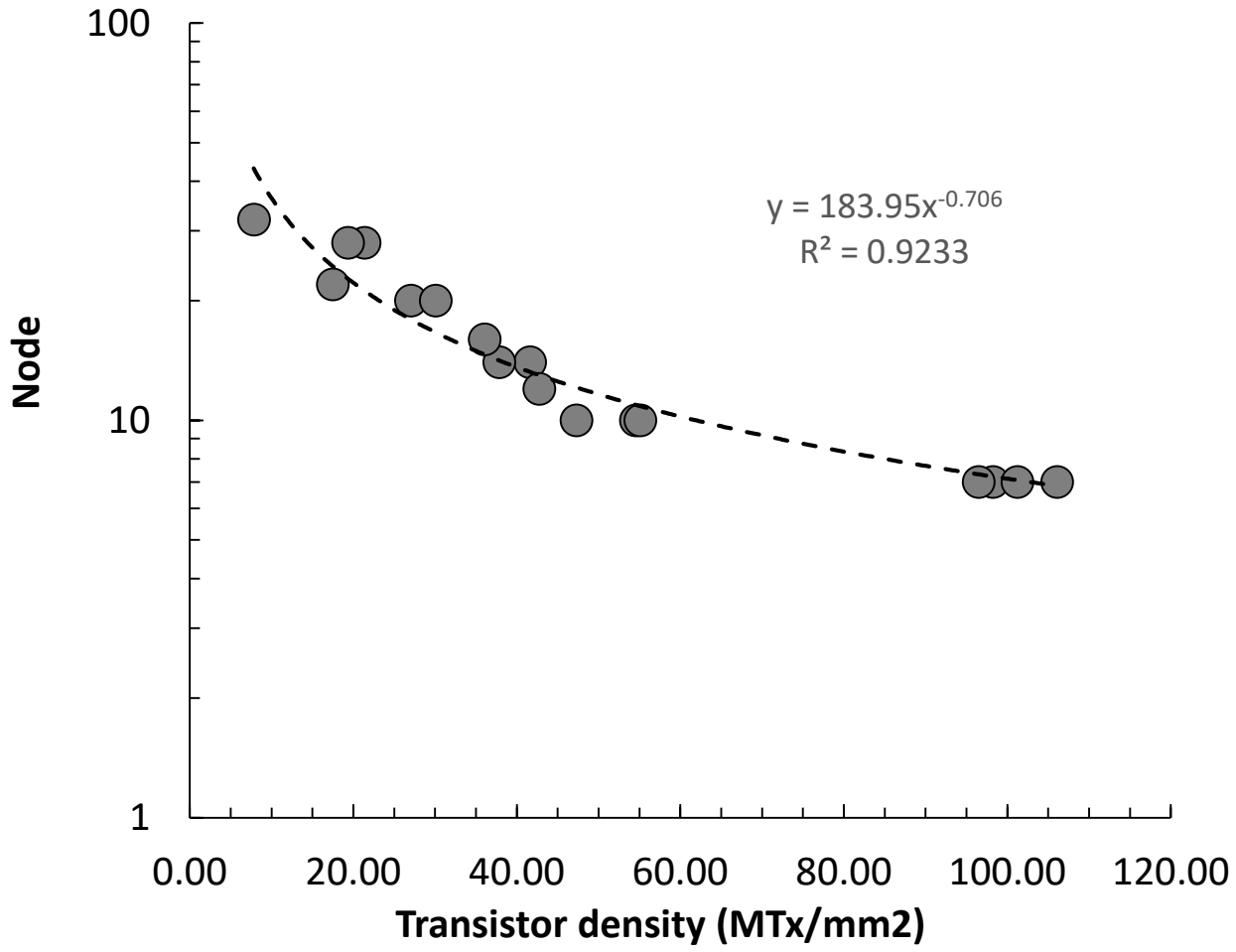
Standard Node Based on Transistor Density

- The plot on the right plots the stated node for technologies versus transistor density for the four leading edge logic companies.
- Only actual values are plotted.



Standard Node Versus Transistor Density

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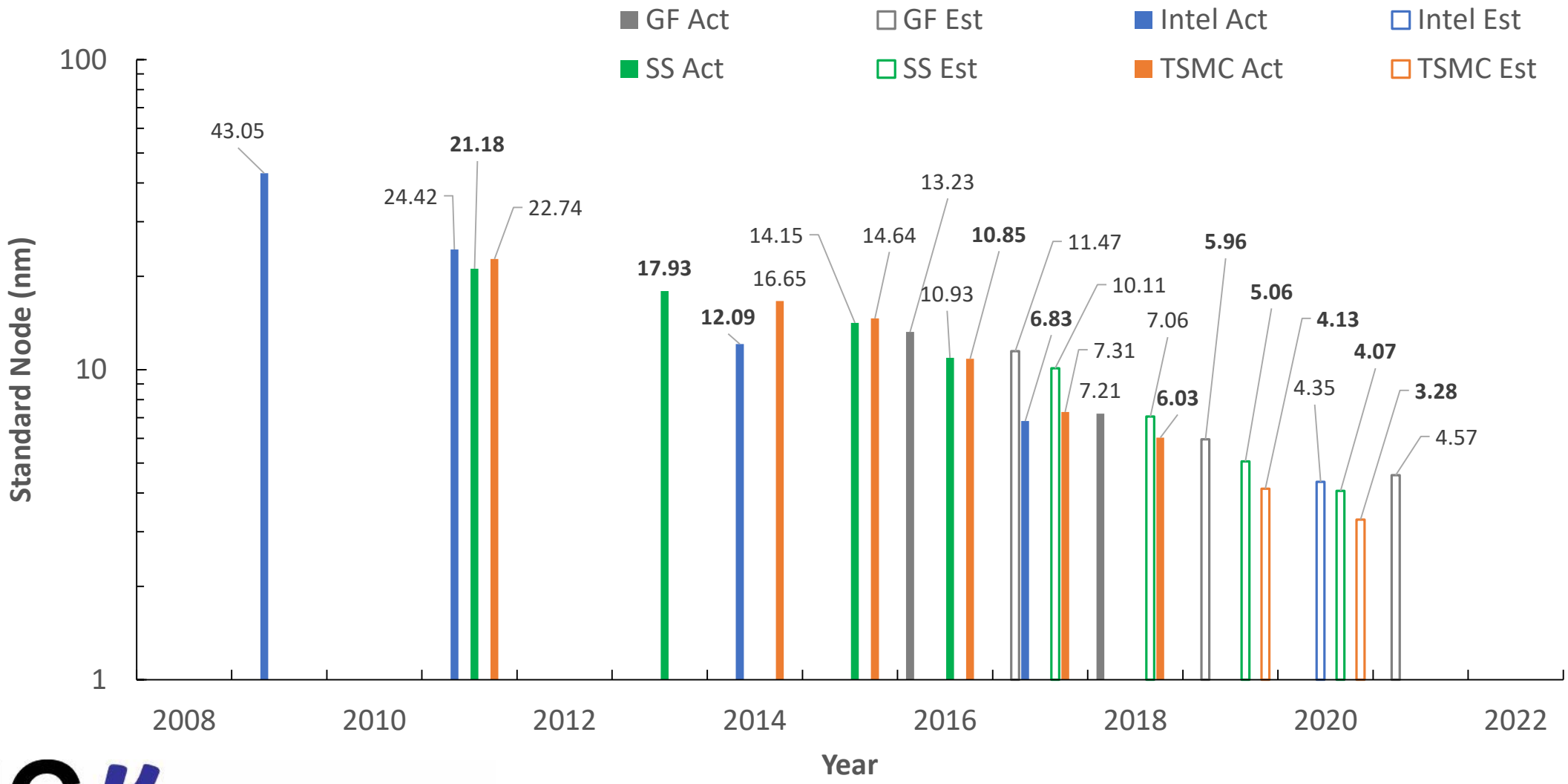
Standard Node Trend



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Conclusion

- A detailed analysis of known and estimated nodes has been performed accounting for M2P, CPP, Tracks and DDB versus SDB.
- A standard node versus transistor density metric has been developed.
- The smallest standard node by year has been calculated and plotted for each of the four leading edge logic producers.
- Accounting for all factor intel has a slight standard node lead in 2017 but we expect TSMC to take the standard node lead in 2018.
- We expect TSMC and Samsung to maintain standard node leads over Intel from 2019 through 2022.