# The Impact of EUV on the Semiconductor Supply Chain

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# Outline

- Why EUV
- Who needs EUV
- EUV adoption roadmaps
- EUV wafer volume projections
- Impact of EUV
- Conclusion

# Why EUV

1. **Cycle time** – a single EUV exposure replaces 3 or more optical exposures. Each exposure takes approximately 1.5 days.
2. **Edge Placement Error (EPE)** – multiple masks to create a pattern increases edge placement error. A single EUV exposure can improve EPE up to 90%.
3. **Pattern fidelity and electrical distributions** – the quality of EUV patterns is better and have shown tighter electrical distributions.
4. **Cost** – probably not a cost reduction at least initially, being done for the first three reasons.

# Who Needs EUV?

- NAND – **No** – NAND is transitioning from 2D NAND that was lithography driven to 3D NAND with relatively large features and layer driven scaling. 3D NAND is driven by deposition and etch, not lithography.
- Logic – **Yes** – 7nm is ramping now with mid 80s mask counts and many multipatterning layers, 5nm will be >100 mask layers with cycles time ~6 months and edge placement error issues. EUV adoption will begin in 2nd and 3rd generation 7nm processes.
- DRAM – **Yes, but logic will go first** – DRAM has manageable mask counts, only a few multipattering layers and is capacitor limited. EUV will likely be introduced for a few layers at some point but will trail logic. Samsung has 1x (18nm) DRAM in production and is ramping 1y without EUV.

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# 7nm Foundry Logic - Generation 1 (7)

- What – optical process, no EUV.
- Who/When
  - TSMC (7FF) – ramps 1H 2018.
  - GLOBALFOUNDRIES (7LP) – ramps 2H 2018.
- Layers - no EUV layers.
- What is needed – nothing, optical technology, ramping now.

| Layer | Pitch (nm) | Lithography |
|---|---|---|
| Fin | 29-30 | SAQP |
| Gate | 56-57 | SADP |
| Contact | ~56-57 | LE3 |
| 1x Metal | 40 1D | SADP |
| 1x Via | ~60 | LE3 |

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# 7nm Foundry Logic - Generation 2 (7c)

- What – EUV for contacts and vias, possibly without a pellicle. Provides no shrink but shorter cycle time.
- Who/When
  - GLOBALFOUNDRIES (7LP) – early 2019.
  - TSMC (7FF) – early 2019.
- Layers - 15 optical layers replaced by 5 EUV layers.
- What is needed
  - High throughput EUV tools with 90% uptime – currently around 75% per Intel at IEDM. ASML has to execute on their plan.
  - High power pellicle if a pellicle is used.
  - Reticle inspection with eBeam, OK but not optimal.
  - Photoresists are probably OK, but dose may be higher than desired at ~30mJ/cm$^2$.

| Layer | Pitch (nm) | Lithography |
|---|---|---|
| Fin | 29-30 | SAQP |
| Gate | 56-57 | SADP |
| Contact | ~56-57 | EUV |
| 1x Metal | 40 1D | SADP |
| 1x Via | ~60 | EUV |

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# 7nm Foundry Logic - Generation 3 (7+)

- What – EUV for contacts and vias with or without a pellicle. 1x metal with a pellicle. Provides a metal shrink from 7c for GLOBALFOUNDRIES and TSMC.
- Who/When
  - Samsung (7LPP) – early 2019 (first 7nm for Samsung).
  - TSMC (7FF+) – mid 2019.
  - GLOBALFOUNDRIES (7LP+) – late 2019.
- Layers - 23 optical layers replaced by 9 EUV layers.
- What is needed
  - Same items as 7c
  - Redesign for GLOBALFOUNDRIES and TSMC.
  - High power pellicle, 90% transmission desirable.
  - Actinic inspection desirable.

| Layer | Pitch (nm) | Lithography |
|---|---|---|
| Fin | 29-30 | SAQP |
| Gate | 56-57 | SADP |
| Contact | ~56-57 | EUV |
| 1x Metal | 36 2D | EUV |
| 1x Via | ~60 | EUV |

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# What About Intel

- Intel 10nm is ramping now. All optical process with similar density to foundry 7+ processes. Intel i10 ~ foundry 7+.
- During an interview with Intel's director of lithography Janice Golda she indicated Intel has not decided on a node for EUV introduction but will introduce it when ready.
- Intel process introductions stretching out, when will 7nm ramp?
- Intel plans 10+ and 10++, I am assuming 10+ for EUV introduction 2019. Intel i10+ similar to foundry 7+.

| Layer | Pitch (nm) | Lithography |
| --- | --- | --- |
| Fin | 34 | SAQP |
| Gate | 54 | SADP |
| Contact | ~54 | LE3 |
| 1x Metal | 36-44 | SAQP/SADP |
| 1x Via | ~60 | LE3 or SADP |

# 5nm Foundry Logic (5)

- What – EUV for 11 to 12 layers with a pellicle. Possible EUV for Fin cuts?
- Who/When
  - Samsung (6LPP/5LPP) – 2019
  - TSMC (5FF) – 2019
  - GLOBALFOUNDRIES – assuming 2020
- Layers - 11 to 12 EUV layers
- What is needed
  - Same items as 7nm.
  - Pellicle must be 90% or better transmission.
  - Actinic inspection highly desirable.
  - Much better photoresist, defectivity improvement and much lower dose.

| Layer | Pitch (nm) | Lithography |
|---|---|---|
| Fin | 20 | SAQP |
| Gate | 45-50 | SADP |
| Contact | 45-50 | EUV |
| 1x Metal | 26 1D | EUV |
| 1x Via | 38 | EUV |

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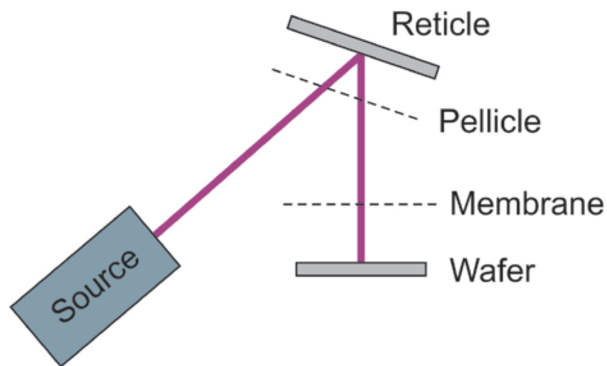
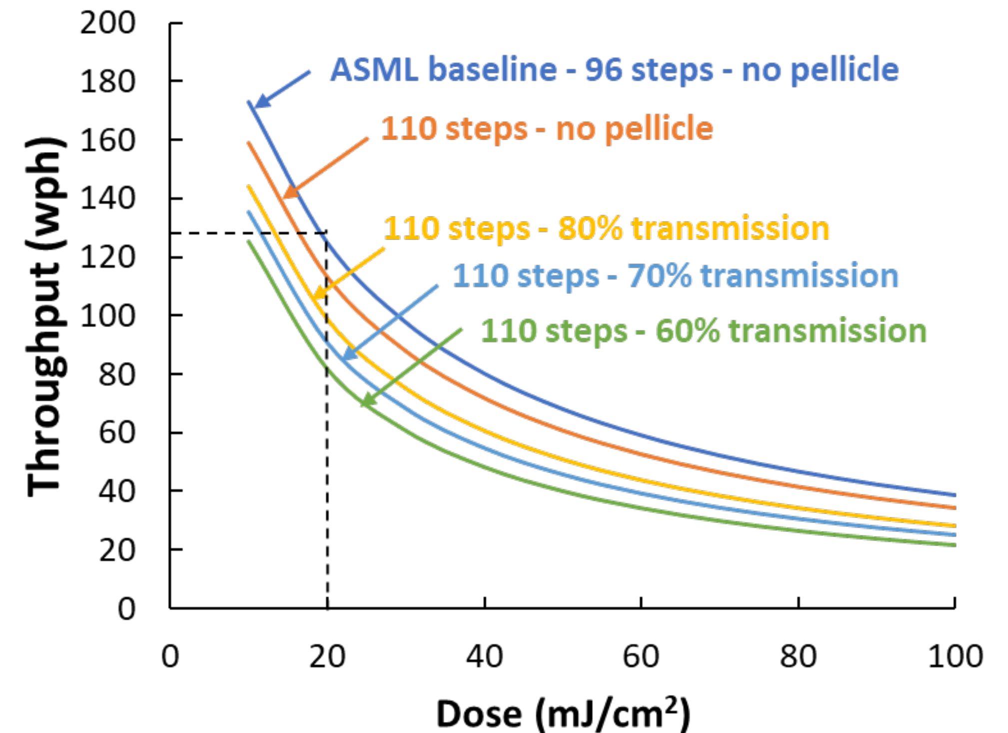
# EUV Throughput

- ASML baseline – 250 watt source, no pellicle, 96 steps, 20mJ/cm$^2$ = (125wph).
- Logic steps ~110.
- Membrane higher transmission than pellicle.




| Pellicle transmission | Comment | Pellicle only | Pellicle + membrane |
|---|---|---|---|
| 83% | Current | 69% | ~60% |
| 90% | Target | 81% | ~77% |

Pellicle Transmission




Throughput Versus Dose

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# Dose and Throughput

- From the previous slide it can be seen that dose has an enormous impact on throughput.
- I have spoken to several lithographers at different companies working on EUV.
- For 7nm foundry the expectation is around 30mJ/cm$^2$.
- For 5nm foundry I had multiple inputs of around 70mJ/cm$^2$. There is significant work that needs to be done on photoresist for 5nm to get this dose down to a reasonable range (<50mJ/cm$^2$) and the work needs to be done quickly to support 5nm process introductions around 2019.

# Wafer Volumes (thousands)

| Process | 2018 | 2019 | 2020 | 2021 | EUV layers |
|---|---|---|---|---|---|
| 7 & i10 | 430 | 970 | 820 | 510 | 0 |
| 7c | 0 | 230 | 180 | 130 | 5 |
| 7+ & i10+ | 0 | 570 | 1,530 | 1,940 | 9 |
| 5 | 0 | 100 | 365 | 1,320 | 11 |
| Total EUV wafers | 0 | 900 | 2,075 | 3,390 | |
| Total WW 300mm logic wafers | 29,574 | 32,694 | 38,454 | 39,774 | |
| EUV % of WW 300mm logic | 0.00% | 2.75% | 5.40% | 8.52% | |
| EUV layers | 0 | 7,380 | 18,685 | 32,630 | |

- The total EUV layers forecast utilizes most of the capacity of ASML's projected EUV tool shipments based on a set of "conservative" throughput assumptions.
- Total 300mm logic wafers is from the IC Knowledge – 300mm Watch database – 2017 – revision 06.
- DRAM will likely start to ramp in 2020 and 2021 and add additional layers.

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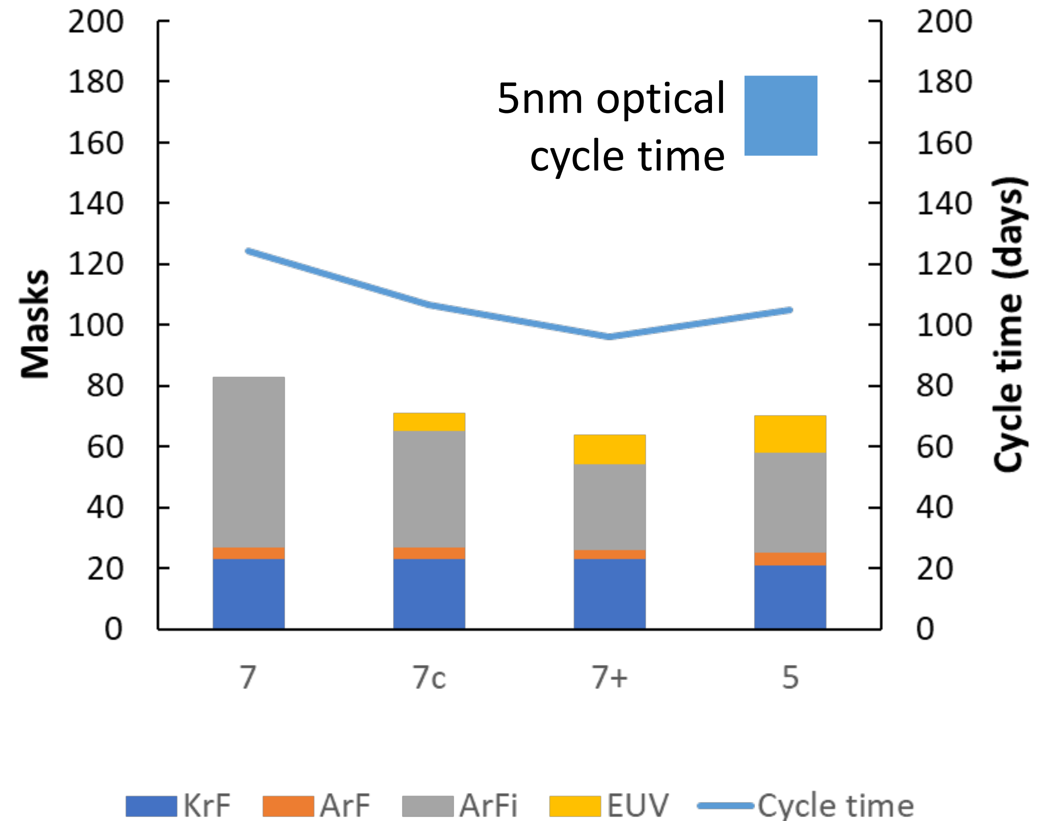
# Masks

- 7 foundry has a 40nm minimum metal pitch (MMP) done with optical SADP and LE3 optical contacts and vias. 7c version uses EUV for contacts and vias only.
- 7+ has a 36nm MMP with EUV for contacts, vias and 1X metal.
- 5nm has 26nm MMP with EUV for contacts, vias, and 1X metal. Possibly EUV fin cut?




**Mask Counts and Cycle Time**

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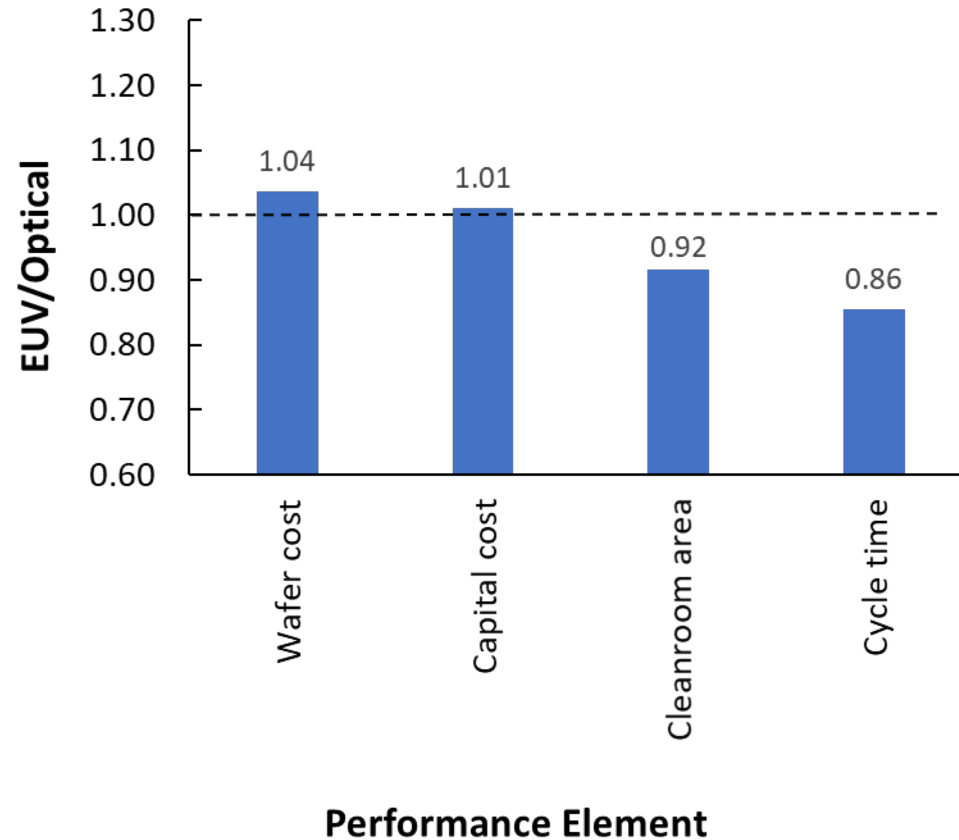
# 7nm EUV Contacts/Vias Versus Multi-patterning

- 40K wpm Fab located in Taiwan.
- Greenfield fab still depreciating.
- 10,000 exposures per reticle, EUV reticle 6X the cost of an ArFi reticle.
- Assumes EUV for 5 contact/via levels at 79wph versus LE3.
- 83 mask optical process, 73 mask EUV process.
- Assuming 250 watts at 90% uptime, we are OK for 7nm contact/via.




**Relative performance of EUV versus multi-patterning**

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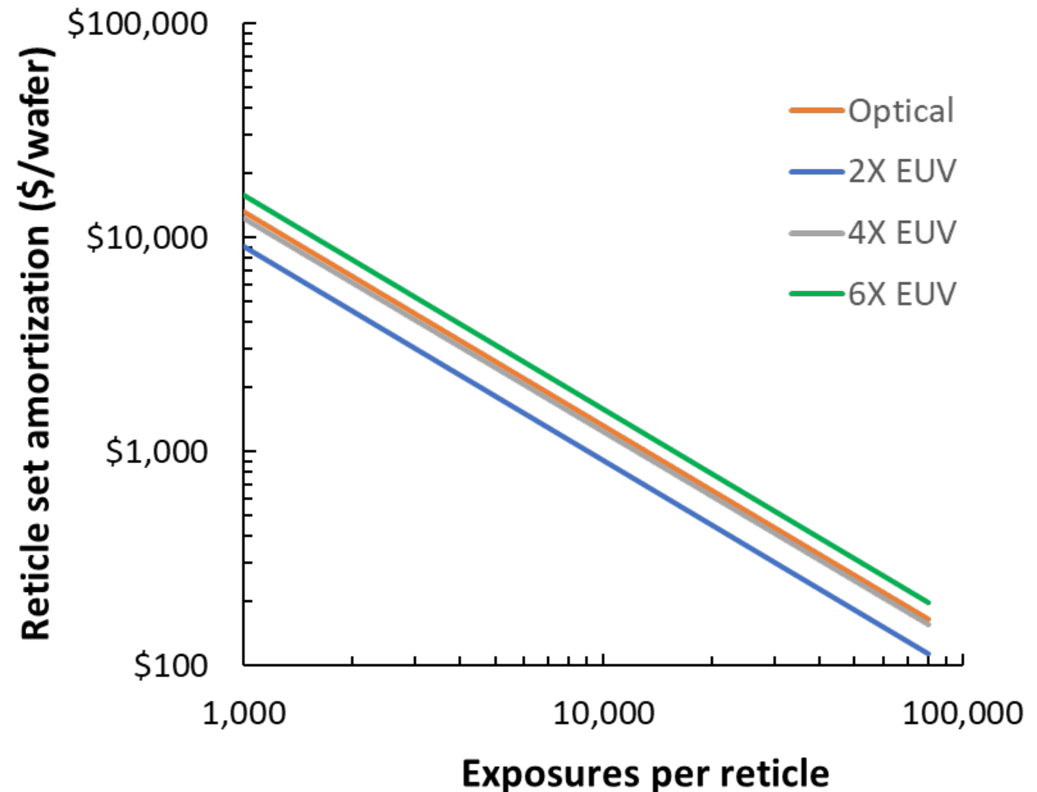
Source: IC Knowledge – Strategic Cost Model – 2017 – revision 05

# Reticle Amortization

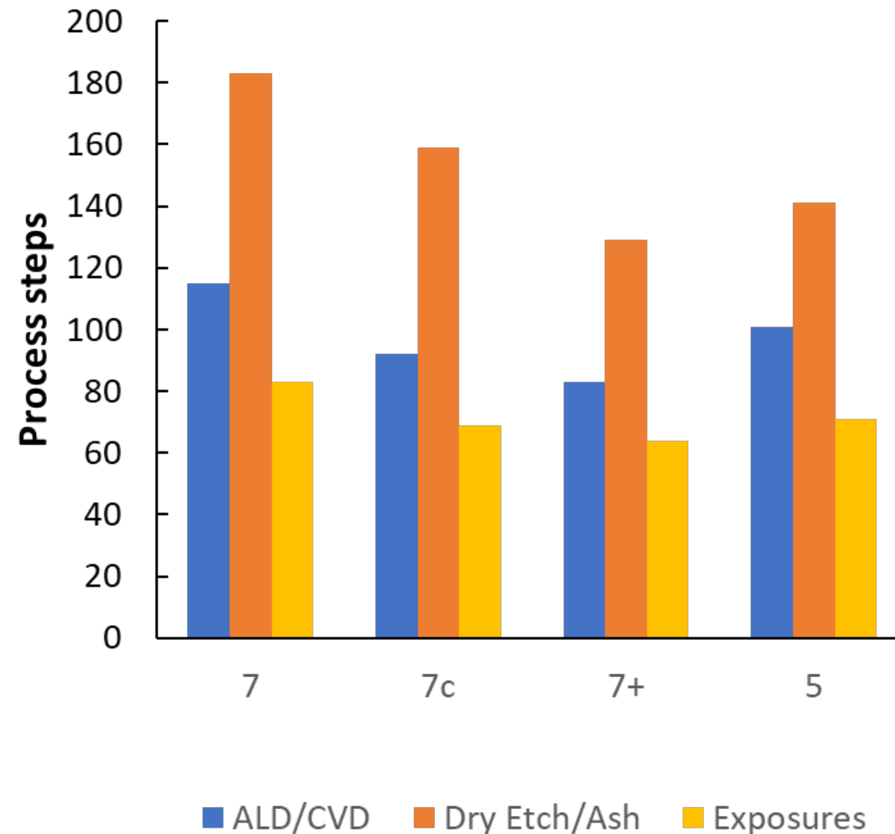
- 5nm Logic process,
- 5nm optical with 111 mask layers, EUV with 70 mask layers
- EUV reticles 2x, 4x or 6x ArFi reticle cost.
- Exposures per reticle as noted.
- Even at 4x the cost of an ArFi reticle, EUV reticle set costs are lower than optical reticle set costs due to fewer reticles.
- 5nm products need to run in high volume (>10K exposures/reticle) to amortize reticle set costs.




Reticle set amortization

# Logic Process Steps

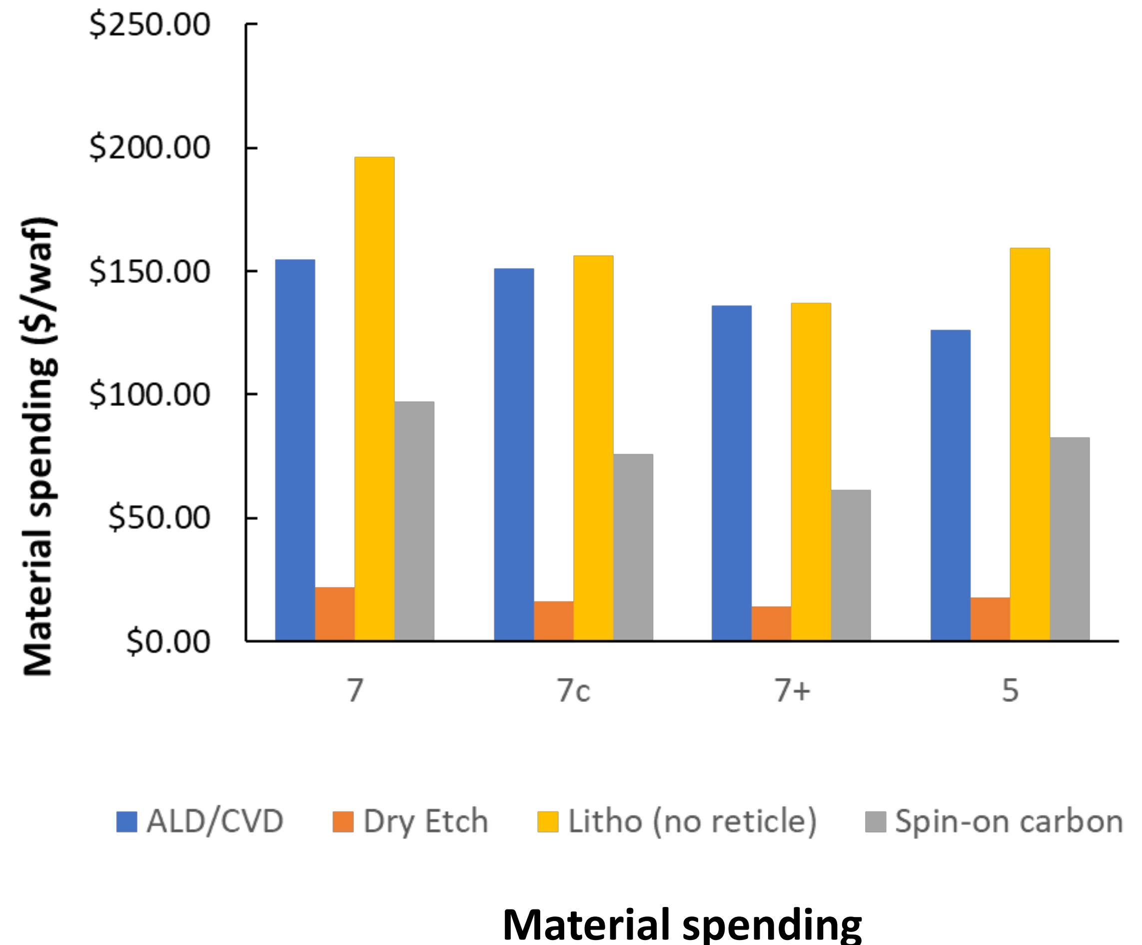
- The implementation of EUV reduces deposition and etch steps versus multi-patterning.
- Overall increases in process complexity moving to 5nm mitigates the effect to some extent.
- 3D NAND increasing layer counts should more than offset the loss in logic opportunity for Deposition and Etch.




**Process steps by type**

# Logic Material Spending

- EUV reduces material spending on deposition, etch and spin-on materials and even lithography materials.
- The move to 5nm mitigate this to some extent.






Source: IC Knowledge – Strategic Cost Model – 2017 – revision 05

# Conclusion

- The major pieces are in-place for EUV adoption for contacts and vias for 7nm logic as long as reasonable uptime is reached. If pellicles are needed a pellicle solution will likely be available in time.
- 7+ with EUV for metal will require a pellicle. A pellicle solution will likely be available in time.
- A lot of work on photoresist is still needed for 5nm. Better pellicle transmission and actinic inspection are both highly desirable.
- The ramp up of EUV will initially be focused on logic and relatively slow. The impact on materials and equipment will be fairly small and likely more than offset by other product segments.

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