PART 1: ANALOG FAULT SIMULATION CHALLENGES AND SOLUTIONS

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SILICON TEST & YIELD ANALYSIS

WHITEPAPER

The quality of an IC test is measured by its fault coverage. For many years, measuring fault coverage has been fully automated for scannable digital circuits, but no comparable measure or automation has been available, until now, for analog tests. This paper (part 1 of a 3 part series) explains why.

A HISTORY

The test time per logic gate in ICs has greatly decreased in the last 20 years, thanks to scan-based design-for-test (DFT), automatic test pattern generation (ATPG) tools, and scan compression. These technologies have prevented Moore's law growth in the number of test vectors applied by automatic test equipment (ATE), while maximizing the coverage of a wide range of defect types.

But for analog circuits[1], **test time per transistor has not decreased** at all. For mixed-signal ICs, test time for the analog portion can dominate total test time. As shown in Figure 1 for mixed-signal automotive ICs, overall **test quality has steadily improved, until recently**. Whenever results asymptotically approach a limit, it indicates that a new tactic is needed to significantly improve results. Figure 1 also shows that test escapes (defects not discovered by test teams) reported by industry are now dominated by defects in the analog portion of ICs, so that is where a **new approach is needed**: better analog tests to improve coverage and more defect tolerance to improve reliability.

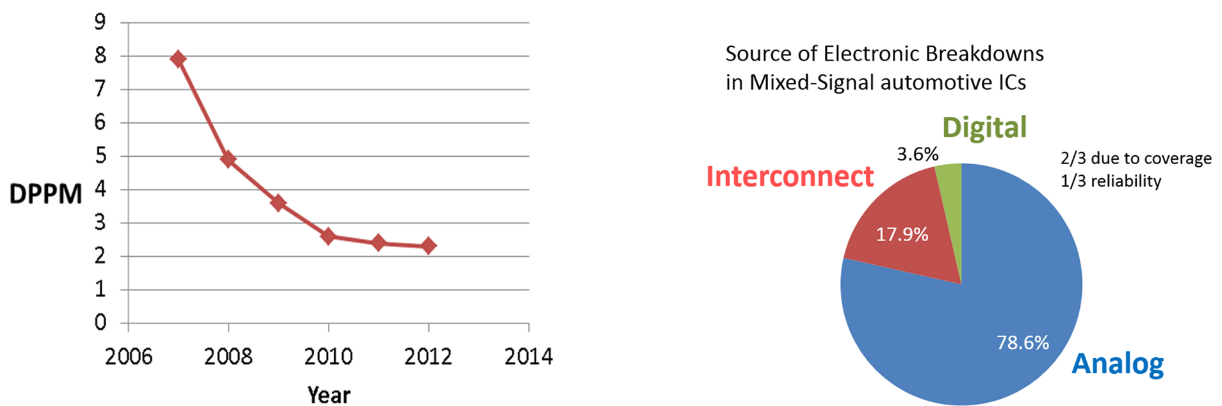

Figure 1: Test escapes (defective parts per million) for a typical automotive IC, and the source of breakdowns [1].

What is not shown in these graphs is the effort and expertise needed to achieve the improvement in analog defective parts per million (DPPM). Analog designers and test engineers do not have DFT tools comparable to those used by their digital counterparts. It has been difficult to improve DPPM because it has been too challenging to measure defect coverage and defect tolerance. These are typically measured by the rate of customer returns, which can occur months after the ICs are tested. This can be expensive for a company. Although fault simulation for digital circuitry was a major EDA tool category in the 1990s, with companies such as Ikos (later acquired by Mentor Graphics) providing hardware accelerators dedicated to the task, it is now embedded within digital ATPG software so that nearly 100% coverage is achieved automatically. Analog fault simulation has only been discussed in academic papers and recently, in a few industrial papers that describe proprietary software.

Why haven't the analog fault techniques described in all those papers produced commercially available fault simulators? Mostly because there is no industry-accepted analog fault model and simulating all potential faults requires an impractically long time.

1 "Analog" has a broad meaning in the IC industry. It includes mixed-signal circuits and usually custom or very-high-speed digital circuits. Meaning, any circuit for which performance, as measured by upper and/or lower test limits, is a key deliverable.

Short circuits are the most prevalent manufacturing defects and comparable to stuck-at faults in digital, but they are too simplistic as an analog fault. Open circuits are common, but a complete open is too difficult to model when it is in series with an MOS transistor gate, and a resistive open in this case usually has no effect because of the much longer time constants in analog relative to digital circuitry. Parametric faults seem much more appropriate for analog, but the list of such faults is almost endless, even before considering combinations.

A limitation of all these fault types is that they each have different likelihoods of occurring. The same is true in digital circuitry, but the variation in likelihoods is much greater in mixed-signal circuits [2]. Theoretically, DPPM must be calculated using likelihood-weighted defect coverage [3], but in digital fault simulation this is overly complicated, so all stuck-at faults are treated as equally likely. As a result, there is only a loose correlation between DPPM and stuck-at fault coverage [4]. To more accurately estimate DPPM, the likelihood of each defect should be included, but this has not generally been practical.

Long simulation time is the most common complaint about designing analog circuitry and simulating faults adds even more simulation time. The number of potential shorts and opens in analog circuit blocks can be very high. For example, layout-extracted netlists often have tens of thousands of parasitic capacitors and resistors, and each one indicates a potential short and open, respectively. The number of potential parametric faults is even larger. Furthermore, some faults are only detectable at a process corner or extreme test condition, for which a designer adds performance margin at the nominal test condition.

Simulating every potential defect, therefore, is impractical unless simplifications are made. Simulators and designers already optimize simulation time versus accuracy as much as possible for a given circuit. Therefore, any further speed up for fault simulation necessarily reduces accuracy and that can result in falsely-detected or falsely-undetected faults. If a designer's diagnosis of an undetected defect concludes that accuracy is to blame, confidence in fault simulation diminishes along with its benefits.

These two challenges, long simulation times and the need for a standard analog fault model, have been targeted in many ways by academia and industry.

POTENTIAL SOLUTIONS FOR REDUCING SIMULATION TIME

Many methods have been proposed over the last 20 years for reducing simulation time per defect. They fall primarily into the following categories:

1. **Simulate only shorts and opens in the schematic netlist**, without variations. Typically, six defects are injected per transistor, and two per passive element. The number of defects can be very high, even though the additional shorts and opens possible in the layout are not included.
2. **Analyze a circuit's layout to find the shorts and opens** that can actually occur (and the likelihood of those defects occurring). Then, create an equivalent in the circuit's netlist, and simulate only those defects [5]. "Inductive fault analysis" uses a circuit's layout and can produce a likelihood-weighted estimate of defect coverage. But, often the layout is not available, the number of potential defects is still large, and variations are ignored.
3. **Simulate only in the AC or DC domain**. AC and DC mode simulations assume that a circuit is linear and they are very efficient for simulating open, short, and variation defects. But, these simulations are unsuitable for mixed-signal circuits such as PLLs. Time domain (transient mode) simulations are suitable for any circuit, but are much slower than AC or DC simulations.
4. **Simulate the sensitivities** of each tested performance to variations in each circuit element [6]. Sensitivity analysis is very efficient in SPICE (similar to AC or DC mode) and any test that detects a variation in a circuit element will also detect a short or open in it. But sensitivities can only be calculated for linear circuits.
5. **Use a simplified, time domain simulation**, such as fault sensitivity analysis (FSA), to measure the impact of injected shorts and opens on output signals only within the same clock cycle. This can reduce simulation time by over 100X but misses the impact of defects that only affect an output in subsequent clock cycles, and this can affect simulation accuracy [2].
6. **Measure the current interrupted by each injected open or flowing through each injected short**, or measure toggle coverage. If the change in current is too small, the circuit's behavior is not changed enough by the defect. This technique only assesses the controllability of a defect: whether the defect is sensitized by the test stimulus and not whether the defect affects an output. Toggle coverage, the percentage of nodes that toggle, is a related metric used for digital circuits but it too only measures controllability.

Even if these techniques are very efficient and reduce simulation time dramatically, the large number of defects simulated means that the number of undetected defects to diagnose will be large. Analyzing each defect is a very time-consuming task that requires detailed knowledge of the circuit and tests.

If there are 100,000 potential faults in a circuit and 90% are detected, there will be 10,000 undetected faults to investigate. Some of the undetected defects are variations that pass marginally and some are in redundant circuitry. Other undetected defects require test modifications, such as tighter test limits (without reducing yield), a different stimulus frequency, or more tests. Some undetected defects might require test access to additional circuit nodes, meaning a change in the design is needed.

In reality, only a small percentage of the 10,000 undetected defects would be investigated before reasons for the coverage loss emerge.

Another way to reduce simulation time is to reduce the number of defects simulated. This also reduces the number of undetected defects to investigate. The methods for reducing the number of defects to simulate include:

1. **Randomly select defects** from a list of all potential defects. This was first used for digital fault simulation where the designer selects a few thousand defects from a list of millions [7]. The mathematics of simple

random sampling is well understood and the confidence interval[2] is easily calculated. When considering defects in mixed-signal ICs though, a relatively small number of defects (perhaps a few thousand) has much higher likelihoods than the others. If the test misses some of these, the coverage estimate could be very inaccurate.

2. **Randomly select defects, after grouping** them according to defect likelihoods [8]. Stratified random sampling, as it is called, groups defects according to their individual likelihoods (based on values such as wire length, number of nodes connected, and area), and ensures that defects are selected from each group (stratum). This improves the confidence interval because there is less variation within each group than across all defects, and the contribution of each group is weighted according to its likelihood and/or variation.
3. **Select only principal parameters** of the circuit elements. A MOS transistor is typically modeled using hundreds of process parameters, but its characteristics are dominated by threshold voltage, gate length, width, oxide thickness, and K'. Simulating defective variations in this smaller number of parameters reduces the number of simulations and eliminates the need to simulate shorts and opens. But the number of defects is still large.
4. **Select representative defects**, based on circuit analysis [9]. For example, if the output of any inverter is stuck-at 1 within a chain of logic inverters, then no signal will propagate through the chain. Simulating a single stuck-at 1 and 0 in the chain is sufficient. In a differential pair of transistors, a high threshold voltage in one of the transistors is equivalent to a low threshold in the other, so only one of the defects must be simulated. So far, this analysis can only be performed manually and thus it is susceptible to analysis errors and the estimation accuracy cannot be calculated.

POTENTIAL STANDARD ANALOG FAULT MODELS

The digital, single stuck-at fault model was proposed about 50 years ago. It has been widely recognized as overly simple but nevertheless has proven to be extremely useful because it is efficient to simulate and because more complex faults, such as transition faults and delay faults, can be modeled using stuck-at faults. No similarly-simple fault model has been accepted for analog circuits.

Simulating only short and open defects has not been accepted because analog design is inherently about tolerating variations and because manufacturing experience has shown that some ICs are defective because of parametric defects. A test that detects all opens and shorts might miss some defective variations.

Simulating defective variations in circuit elements has not been accepted because to achieve acceptable yield, designers already use Monte Carlo simulations to ensure a design can meet all specifications in the presence of all expected variations in process, voltage, and temperature (PVT). Semiconductor wafers contain process control monitors (PCMs), which are small standard circuits on the wafer for measuring to ensure process parameters across the wafer are within specification. As a result, **most defects seen in manufactured ICs are shorts and opens** (except in the most advanced process nodes).

In view of the lack of an industry-accepted fault model, a group of about a dozen companies (including Mentor Graphics) has been meeting regularly since mid-2014 to develop such a fault model. The group has reported their progress publicly several times [10], and they hope to develop an IEEE standard by 2018.

Simulating defective variations in high-level models of basic analog functions (such as op-amps, filters, and ADCs) has not been accepted because there is no way to delineate a sufficient set of defects, the defects do not correlate to silicon defects, and creating these models and defective variations is a difficult and non-automated task.

2 The confidence interval is the variation in an estimate that would occur if the random sampling was done many times. It is typically stated as, for example, within ±3%, 19 times out of 20.

THE TESSENT DEFECTSIM SOLUTION

Some companies have experimented with analog fault simulation and have specific fault models and DFT strategies in mind that they want to implement in commercially-available software. Other companies simply want to improve analog test coverage or test time using an approach that is best-in-class compared to all published approaches.

Tessent® DefectSim™ incorporates lessons learned from all previous approaches and combines the best aspects of each, while avoiding their pitfalls. Simulation time is reduced using a variety of techniques that combine to reduce total simulation time by many orders of magnitude compared to some of the previous approaches, without introducing a new simulator or reducing existing simulator accuracy. The analog fault model can be shorts and opens, just variations, or both. Or, designers can substitute their own proprietary fault models. The defects can be injected at the schematic level, at the layout level, or a combination of both.

REDUCING SIMULATION TIME

Likelihood-weighted random sampling (LWRS) minimizes the number of defects to simulate [10]. This is a new statistical technique, equivalent to stratified random sampling in which each stratum contains only one sample (defect). The likelihood of randomly selecting any given defect is proportional to the likelihood of the defect occurring. Each likelihood of occurrence is computed based on designer-provided global parameters, and parameters of each circuit element. For example, shorts are "the most dominant" [2]. In state-of-the-art production processes, shorts are 3~10X more likely than opens. When the range of defect likelihoods is large, as it is for mixed-signal circuits, LWRS requires up to 75% fewer samples than simple random sampling (SRS) for a given confidence interval, as Figure 2 shows. In practice, when coverage is 90% or higher, this means that it is usually sufficient to simulate a maximum 250 defects, regardless of the circuit size or the number of potential defects, to estimate coverage within 2.5%, for a 99% confidence level. Simulating as few as one hundred defects is sufficient to get ±4% estimate precision. For small circuits, or when time permits, all defects can be simulated.

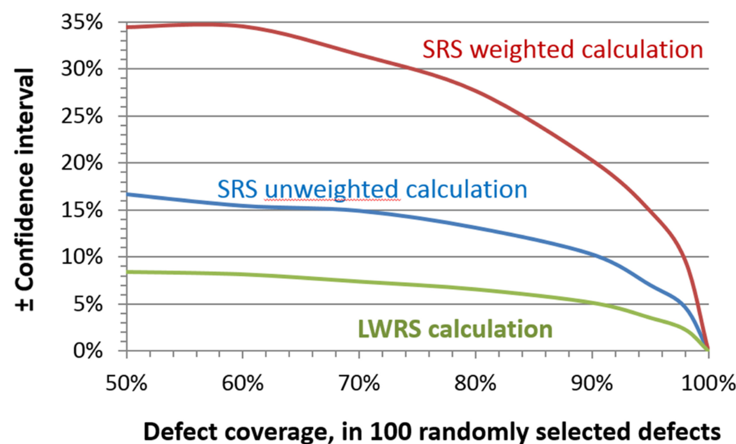

Figure 2: 99% confidence interval, for estimate based on a sample size of one hundred defects[11].

DefectSim automatically substitutes the highest model or netlist available for each subcircuit instance that does not contain the defect being simulated. The lowest netlist available for each subcircuit is used to find the potential defect sites and each defect is injected into that netlist. This ensures that when layout-extracted netlists are available, defects are based on the layout. This approach requires the simulator to re-load most or all of the circuit for each defect being simulated. But this is automatic and the time is insignificant compared to total simulation time. When hardware description language (HDL) models are available, in Verilog-A or Verilog RTL for example, they can reduce simulation time by one or two orders of magnitude. In practice, the highest level netlist is often just the

schematic, but it typically simulates an order of magnitude faster than the layout-extracted netlist. DefectSim runs Eldo® when the circuit contains only SPICE and Verilog-A models, and Questa® ADMS™ when Verilog-AMS or RTL models are used (Figure 3).

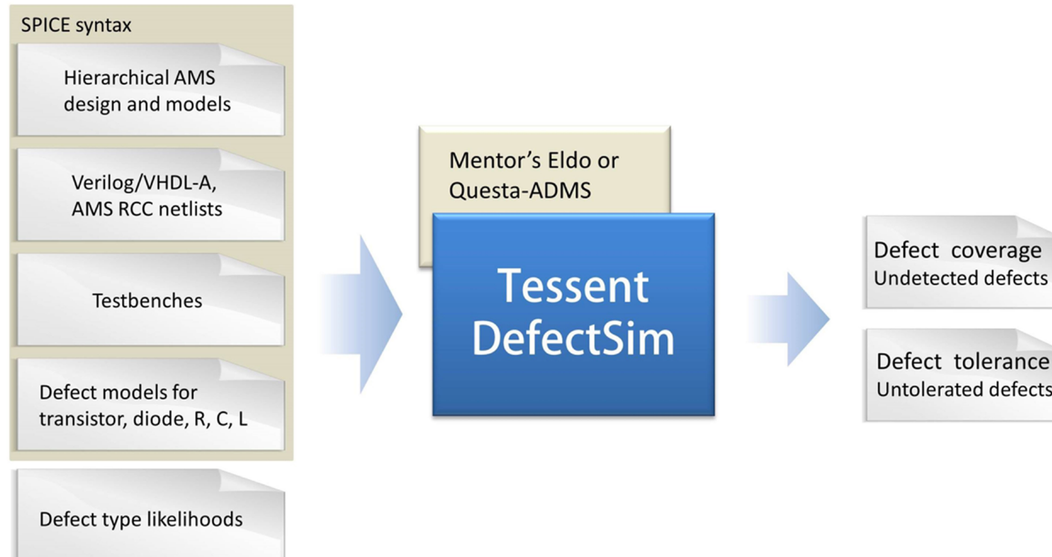

Figure 3: DefectSim flow overview.

Stop-on-detection minimizes simulation time for each defect. As soon as a defect is detected within a simulation, its particular simulation is stopped. To reduce time further, DefectSim automatically simulates only the defects undetected by previous testbenches in each additional testbench. It also simulates at process corners only the defects undetected for the 'typical' process.

For linear circuits, AC and DC mode simulations are most efficient. But, for many mixed-signal circuits, time domain (transient mode) simulation is necessary. DefectSim allows the designer to simulate in any of these modes and any combination.

DefectSim compares the voltage across the injected defect to the voltage before the defect was injected (similar to toggle coverage), and reports this to help designers diagnose whether a defect is undetected because the voltage across it has not been controlled by the test or because it has not been observed by the test.

Based on their experience and the particular circuit being simulated, designers always choose a combination of simulator settings that make an acceptable trade-off between simulation speed and accuracy. DefectSim permits any of these settings and does not affect them.

To measure coverage, a circuit is simulated for each defect, one at a time, while the tested performances are compared to test limits and digital output values are compared to those of the defect-free circuit. A test failure means that the defect is detected.

Simulation of the defects on parallel CPUs and multi-threading are supported without restriction, the same as for defect-free circuits, but parallel simulation can be more efficient for defect simulation. During defect simulation, each CPU simulates independently of the others because each CPU simulates a different defect. But during defect-free simulation, CPUs must run in lock-step because they are simulating different portions of the same circuit.

Thus, DefectSim allows you to combine almost all of the previously-published techniques for reducing simulation time, including random sampling, high-level modeling, stop-on-detection, AC/DC mode, and parallel simulation. All together, these techniques can reduce simulation time by up to six orders of magnitude compared to simulating the production test of all potential defects in a flat, layout-extracted netlist.

AN INDUSTRY-ACCEPTED ANALOG FAULT MODEL

Until the industry agrees on a single fault model, each company will undoubtedly use whichever fault model that it deems acceptable. DefectSim can use almost any fault model and the model can depend on whether the defects are injected at the layout level or the schematic level.

LAYOUT-EXTRACTED NETLIST FAULT MODEL

In layout-extracted netlists, DefectSim injects one defect per parasitic capacitor or resistor representing a potential short or open, respectively. Figure 4 shows two example parasitics.

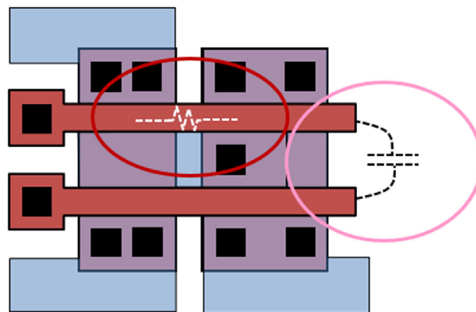

Figure 4: A layout showing a series parasitic resistance in a polysilicon connector and a parasitic capacitance between two nodes.

Each extracted parasitic capacitor indicates two conductors in close proximity and the capacitance is proportional to the distance for which the two conductors are adjacent and inversely proportional to the distance between the two conductors. The likelihood of a short between the two conductors typically has the same dependence.

DefectSim models a short circuit as a resistor. Any resistance that is significantly lower than the impedance of most of the circuit's nodes can be considered a short circuit. Lower values are easier to detect: any test that can detect a 10k ohm short can also detect lower resistance shorts. On the other hand, lower resistances might be more likely. Simulating N different resistances would be the safest approach, but this increases simulation time by a factor of N. A practical compromise it to use a single resistance value between 50 and 5000 ohms.

Each extracted parasitic resistor indicates either a relatively long/thin conductor, or a via. In any case, it represents a potential open circuit and the likelihood of an open is proportional to the resistance. Of course, the resistances of polysilicon and diffusion levels are much higher than for metal levels, so the likelihood is mask level dependent. The level is often reported by layout extraction software as a comment in the netlist, which is ignored by the simulator but not by DefectSim.

DefectSim models an open circuit as a series resistor, plus a leakage resistor at each end of this resistor connected to a randomly-selected power rail. This ensures that no MOS transistors will have an undefined gate voltage and it models leakage that is likely to occur.

DefectSim allows the designer to choose any resistance for the short and open and to define different fault models. The designer can also define the defect likelihood equations. Within a layout-extracted netlist, only resistances and capacitances less than designer-set maximum values are treated as parasitics. All others are treated as design-intent.

SCHEMATIC NETLIST FAULT MODEL

In a schematic netlist (the design-intent), DefectSim injects two defects per circuit element: excessive increases and decreases in the passive elements (R, C, L) and stuck-on and stuck-off in the transistors and diodes. The increases and decreases are set by the designer and are not usually equal in magnitude. The likelihood of increasing or decreasing is also set by the designer and they are typically different too. It is very unlikely that a capacitance would increase by 50% but an open in an array of capacitors could decrease its capacitance by 50%.

Five of the six classic defects in an MOS transistor (3 shorts, 3 opens) cause it to be stuck-on or stuck-off. The one exception (sometimes) is a gate-to-drain short. Connecting a gate to drain occurs commonly in analog designs, so detecting it is less important. The advantage of simulating only stuck-on and stuck-off defects is that these defects obviously must be detected, yet coverage of them is often much less than 100%. Some companies report that many of the analog circuit defects observed in customer-returned ICs could have been modeled as stuck-on/off transistors.

DefectSim allows the designer to choose custom defect models. This means that variations in transistor parameters could be injected instead of simple stuck-on/off. For example, instead of stuck-on, a low threshold voltage and 50% wider gate could be injected. Or, instead of stuck-off, a high threshold voltage and 50% longer gate could be injected. Any test that identifies these two defective models will detect all six possible shorts and opens in a transistor.

Thus, DefectSim allows the designer to use any of the classic defect models or create his/her own to specify shorts, opens, and variations of these models.

CONCLUSION

Analog fault simulation is needed to achieve defect coverage and DPPM levels in the analog portion of mixed-signal ICs that is comparable to that in the digital portion. Many analog fault simulators have been proposed by academia in the last 20 years, but none are commercially available for primarily two reasons: impractically long simulation time for industrial circuits and the lack of an industry-accepted analog fault model.

Tessent DefectSim incorporates the best aspects of the previously-proposed approaches to analog fault simulation, without their crucial drawbacks. Simulation time is reduced by a combination of many proven techniques instead of relying on a single technique. Multiple defect models are used, including designer-defined models, and they can depend on whether the defect is injected at the schematic or layout level.

REFERENCES

[1] G.Gielen, W. Dobbelaere, R. Vanhooren, A. Coyette, B. Esen, "Design and test of analog circuits towards sub-ppm level," *Int'l Test Conf.*, 2014

[2] B.Kruseman, B.Tasic, C.Hora, J. Dohmen, H.Hashempour, M. van Beurden, Y. Xing, "Defect Oriented Testing for Analog/Mixed-Signal Designs," *IEEE Design & Test*, Sept./Oct. 2012

[3] J.Teixeira de Sousa, F.Goncalves, J.Teixeira, C.Marzocca, F.Corsi, T.Williams, "Defect Level Evaluation in an IC Design Environment", *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, vol. 15, no. 10, pp. 1286-1293, October 1996

[4] P. Maxwell, R. Aitken, "The effect of different test sets on quality level prediction: When is 80% better than 90%?" *Proc. of Int'l Test Conf.*, 1991

[5] F.Ferguson, J.Shen, "Extraction and Simulation of Realistic CMOS Faults using Inductive Fault Analysiss," *Proc. of Int'l Test Conference*, 1988

[6] S.Khaled, N.Hamida, D.Marche, B.Kaminska, "LIMSoft: Automated Tool for Sensitivity Analysis and Test Vector Generation", *IEE Proc. on Circuits, Devices and Systems*, pp.386-392, December 1996

[7] V.D.Agrawal, H.Kata, "Fault Sampling Revisited," *IEEE Design & Test of Computers*, 1990

[8] F.Goncalves, J.Teixeira, "Sampling Techniques of Non-Equally Probable Faults in VLSI Systems," *Proc. of VLSI Test Symp.*, May 1998

[9] E.Yilmaz, A.Meixner, S.Ozev, "An Industrial Case Study of Analog Fault Modeling," *Proc. of VLSI Test Symp.*, 2011

[10] Emerging Test Strategies Session: "A framework for automation in analog/mixed-signal DfT and test," *European Test Symp.*, 2015, 2016

[11] S. Sunter, K. Jurga, P. Dingenen, R. Vanhooren, "Practical random sampling of potential defects for analog fault simulation," *Proc. of Int'l Test Conf.*, Oct. 2014

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