MobilFlex
Making the PC a PDC

"LAN of Things" Chipsets and PDC – Personal Data Center

Requirements for "proof of concept" prototype

LAN of Things I/O Co-Processors and Chipsets are advanced I/O sub-systems (SOC's) that:

a) Complete the infrastructure on the last thirty yards,

b) Eliminate all I/O limitations and bottlenecks in x86 architecture,

c) More than triple x86 architecture "horsepower" with no increase in manufacturing cost.

This is the most significant improvement to x86 architecture improvement since its introduction 35+ years ago.

They make the currently flat and inefficient x86 architecture, a vertically layered architecture with high degree of concurrency, flexibility and scalability (just like mainframes).

Features and benefits

- Up to 80% more compute power (based on a 4-cores system)
  - Allow up to 100% cpu utilization (like mainframes);
  - Support up to three users or virtual machine per core (like mainframes);
- Up to 16 concurrent M2M between any connected devices, regardless of their native communication protocol and medium, without any performance degradation;
  - Up to four HD video streams and unlimited audio, and data;
  - Sufficient connectivity for any home, office or industrial environment;
- Significant security improvements.
- Customizable for a wide variety of environments, use cases and applications.

Co-Processors vs. Chipset – see block diagrams below

- ***"LAN of Things" Co-Processors*** are classic "add-on" functionality, with minimal impact on the existing software stack, but also with less performance improvements.
- ***"LAN of Things" Chipsets*** replace currently brainless chipset making x86 a micro-mainframe, with proprietary improvements:
  - Proprietary connectivity layer creates the "LAN of Things" and eliminates I/O limitations and bottlenecks;
  - Offloads processing overhead from main cpu and executes it concurrently;
  - Significant security improvements
  - Allows meaningful differentiation and customization;
  - Creates a new class of affordable hardware platform (multi-user, multi-functional) for consumers IOT, edge/fog computing, high density servers, etc.
    - PDC idea and prospect interests many potential customers, partners and investors.
      - They are asking for a "proof of concept"
      - NSF-SBIR is interested to finance the POC, we must submit a full project proposal, with budget and detailed plan of action.

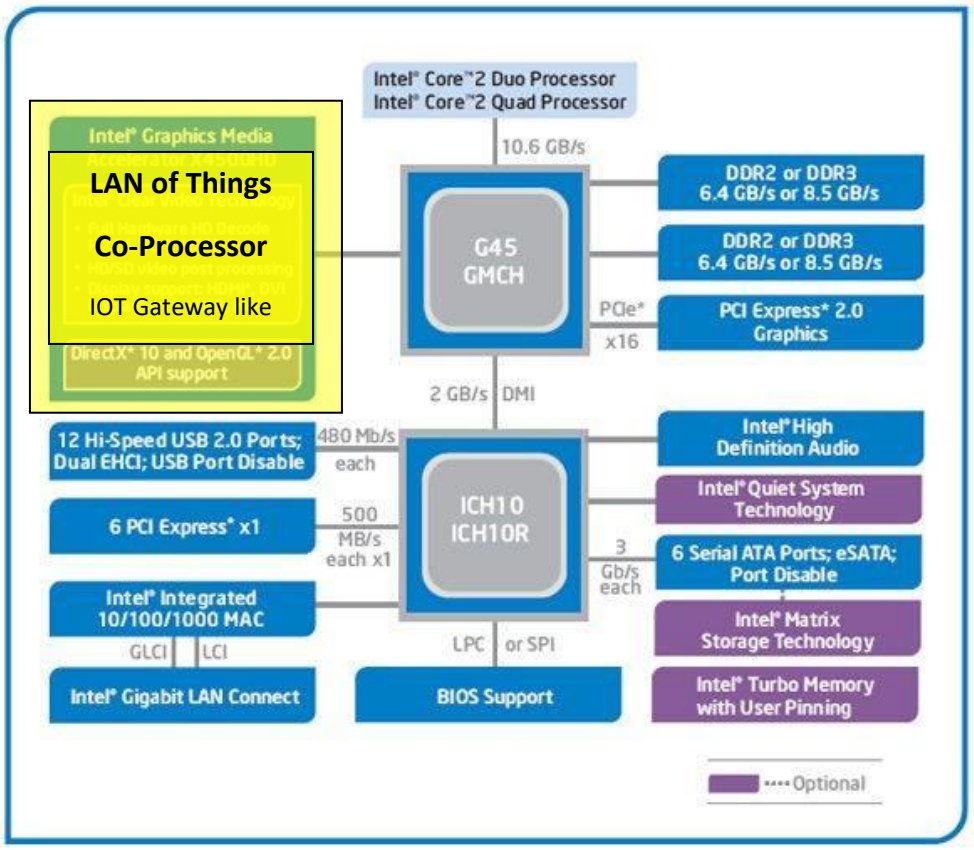
PDC – POC - PRD

The POC must demonstrate that the claims we make about improving x86 performance are true and valid.

While our base product is the “LAN of Things” SOC (the yellow squares in the block diagrams below), we must setup an entire x86 system and submit it to a series of benchmark tests.

- There are countless solutions to design and test the SOC itself (simulation model, FPGA prototype), we are searching for a solution for the rest of x86 system (preferred simulation model).

“LAN of Things” as Co-Processor



"LAN of Things" Chipset

Replaces South Bridge & Connectivity