

flow. To address this issue, we show a SAQP SAV & SAB (SAVB) process in Fig. 11, which can be applied to fabricate the metal track (e.g., M0) of a logic/SRAM cell. Actually, this process can also accommodate direct metal etching based self-aligned cuts (SAC) which, however, may not be introduced to the future nodes (e.g., 19nm metal pitch) accessible with the SAQP technique. The top views of SAB steps are not shown in the figure, readers who hope to know more about the SAB technical details are referred to the published literature (e.g. [26-27]). Assuming the power rail/ground CD is $3F$ (F : the minimum metal half-pitch) and a metal track requires 5 or 3 signal wires, the ratio of (lithographically defined) logic 5-signal-wire mandrel pitch to the minimum metal pitch is 4.5, while the ratio of 3-signal-wire mandrel pitch to the minimum metal pitch is 5. It allows us to use 193i DUV lithography to shrink the minimum metal pitch of M0 to about 17nm. We can see that any pair of neighboring metal wires are covered by two different dielectric hard masks, which provides the etching selectivity and thus rigorous self-alignment for the upward connected vias. Another characteristic of this SAQP SAVB process is its metal-layer division (MLD) capability to split the neighboring metal wires into two vertically staggered layers with their coupling capacitance significantly reduced. The original idea of self-aligned layer division to control the electrostatic capacitance can date back to a MEMS process [42-44] to fabricate a vertical comb-drive structure shown in Fig. 12.

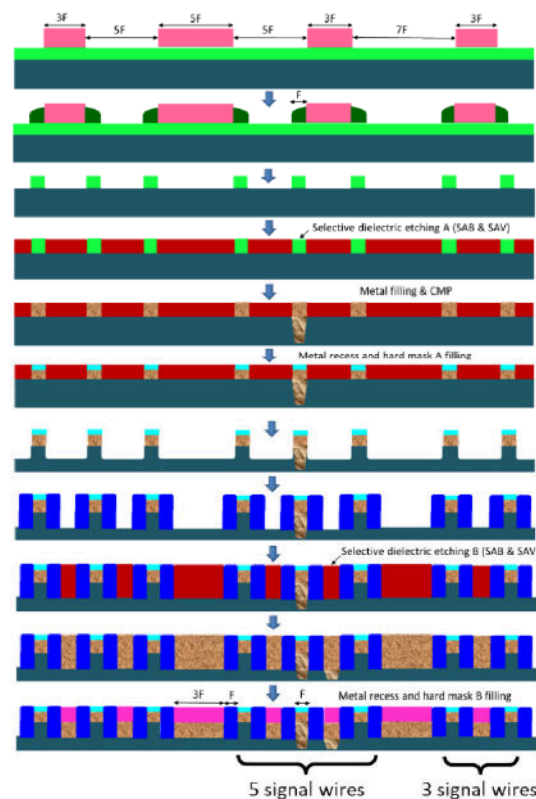


Fig. 11. A schematic demonstration of a SAQP SAVB process which can be applied to fabricate the 5 & 3-signal-wire metal track (e.g., M0).

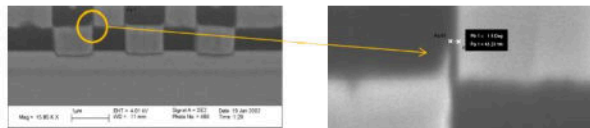


Fig. 12. The layer-division concept demonstrated in a self-aligned MEMS vertical comb-drive structure fabricated using a GCA stepper (resolution $\sim 1 \mu m$). The comb gap was about 40nm (right picture) [42].

In Fig. 13, a 5-signal-wire self-aligned vias & cuts (SAVC) logic BEOL process [45] based on direct metal etching and self-aligned sextuple patterning (SASP [18-19]) is proposed. It is clear that steps (1)-(4) are simply a self-aligned triple patterning (SATP) process for density multiplication, which can be developed separately from the metallization process. Steps (5)-(14) can be considered as a self-aligned double patterning (SADP) process. For the global

semiconductor industry with access to the most advanced EUV scanners, the SATP process module can be skipped and the trench layer shown in step (5) can be directly patterned using EUVL. The top views of SAC steps are not shown in the figure, readers are referred to the published literature (e.g. [35]) for its technical details. Assuming the power rail and ground CD to be $3F$, the ratio of 5-signal-wire logic mandrel pitch ($14F$, lithographically defined) to the minimum metal pitch ($2F$) can be as high as 7 (significantly better than the ratio of 4.5 achievable by a SAQP based SAVB process, see Figs. 11 & 13). It enables a DUV 193i based logic BEOL metal pitch of $\sim 12\text{nm}$. Similarly, a 3-signal-wire SAVC process can co-exist by Spacer2 merging & spacer CD trimming to enable a DUV 193i based BEOL metal pitch of $\sim 16\text{nm}$. Namely, the ratio of 3-signal-wire mandrel pitch to the minimum metal pitch is about 5 (same as achievable by a SAQP SAVB process). In Table 2, we show the superior scaling capability of SAVC patterning process that allows us to use 193i DUV lithography to shrink the minimum metal pitch at least down to 1nm node. Here, the stagnant scaling of metal pitch due to the introduction of buried power rails (BPR) is not considered; rather, a somehow relaxed but continuous node scaling pace is assumed.

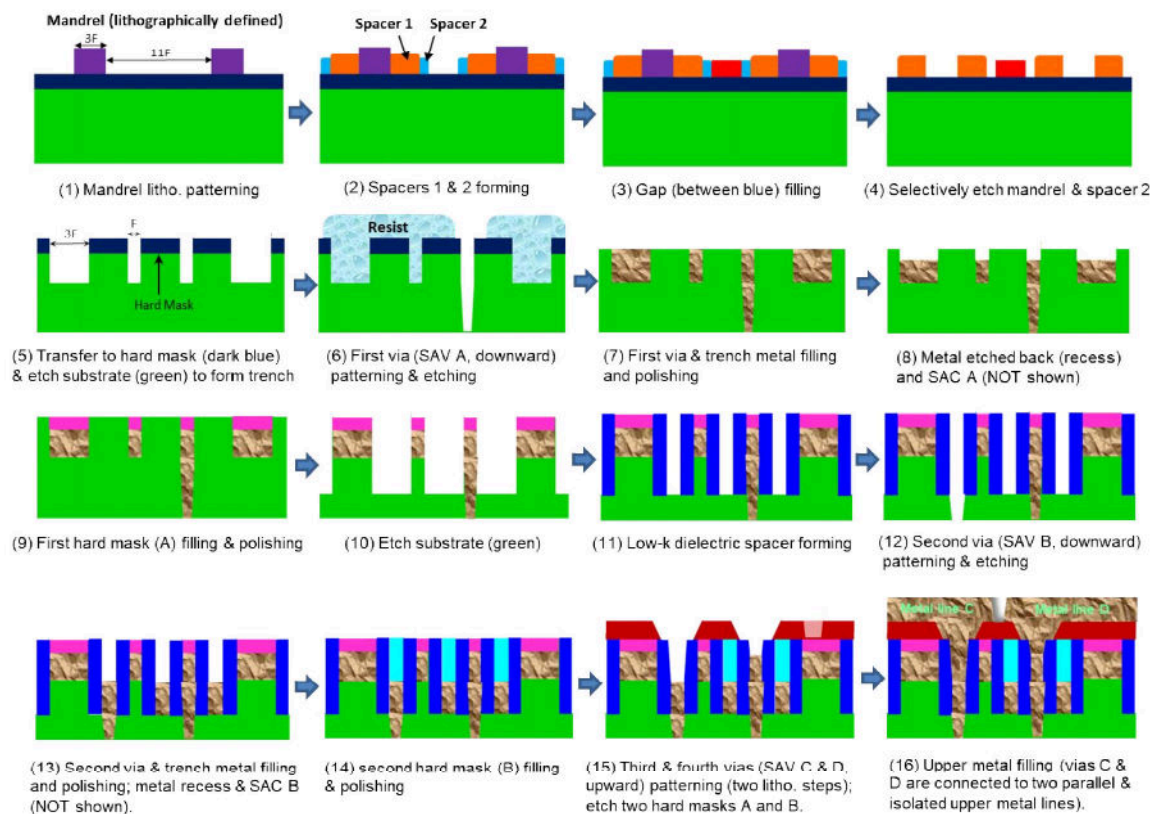


Fig. 13. A schematic demonstration of a 5-signal-line logic SAVC process [45].

CD \ Node	5nm	4nm	3nm	2nm	1nm
Litho. Pitch (nm)	196	168	140	112	84
Min. Metal Pitch (nm)	28	24	20	16	12
Power Rail CD (nm)	42	36	30	24	18

Table 2. The scaling capability of SASP SAVC patterning process.

The idea of metal-layer division can be better understood in a simplified Ru SAVC grating process flow (NO downward SAV) schematically demonstrated in Fig. 14. Sacrificial release of low-k dielectric and the second hard mask (B) will result in two vertically staggered metal layers similar to the vertical comb-drive MEMS structure shown in Fig. 12. In our experiment, the low-k dielectric layer is replaced by ALD oxide. The preliminary experimental result