

EUV MASK TECHNOLOGY AND ECONOMICS: **IMPACT OF MASK COSTS ON PATTERNING STRATEGY**

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MAIN INDUSTRY CHALLENGES

Long term, reliable, high-power source

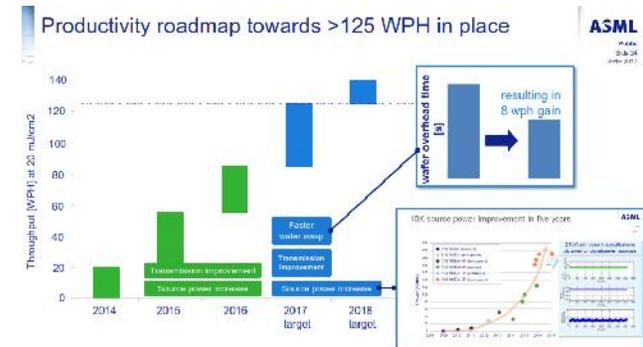
- Demonstrating >100 WPH and >1500 WPD

Improved resists

- Resolution and LWR to meet patterning requirements
- Increased sensitivity can help enable throughput

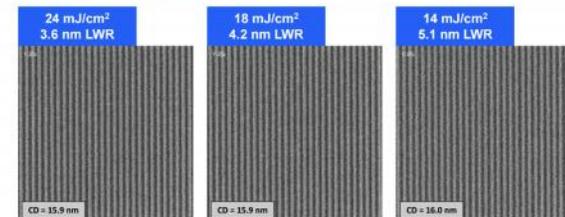
Defect free blanks/masks

- Infrastructure and capability solutions for blank, pattern and mask image inspection



M. Van den Kerkhof., 2017 SPIE AL

16nm HP below 20 mJ/cm²



Meyers, S., 2016 EUVL Workshop

EUV MASK PROGRESS

SNAPSHOT

Blank Defects

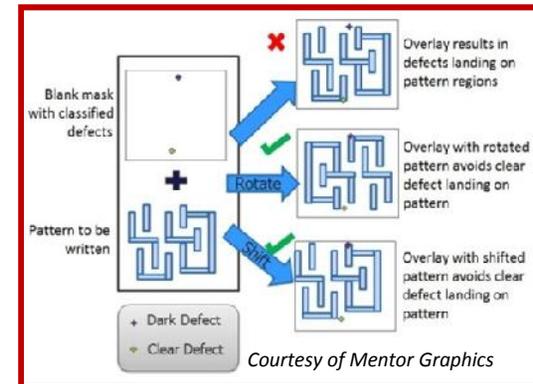
- Blank inspection not gating factor – ABI is available
- Defect compensation and phase defect repair techniques

FEOL Module

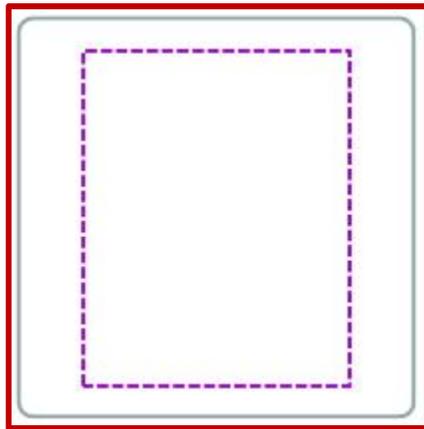
- Patterning capability is not limiting for N7

Mask Border Leakage

- Optimization of dark border process
- Absorber and flare interactions

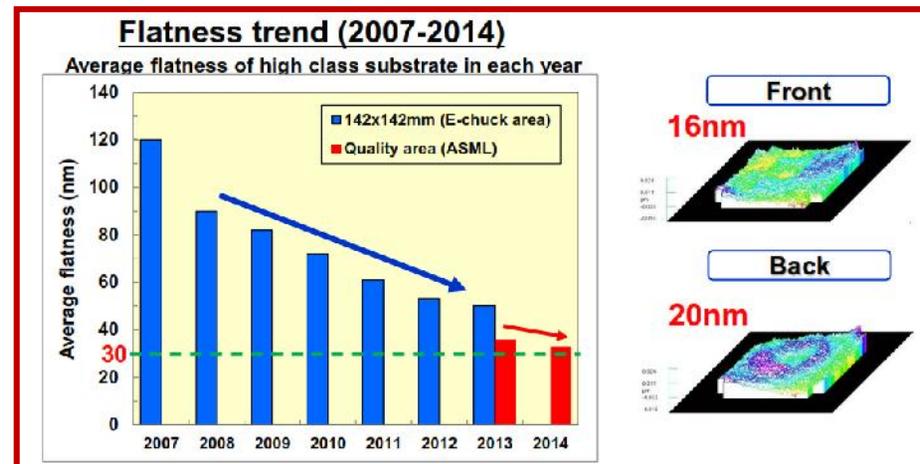


EUV BLANK IS KEY TO SIMPLIFIED INTEGRATION



0 defects @ 23nm SEVD
Demonstrated in 1Q16
132 x 104mm

Onuo, EUVL Symposium 2016, Hoya



Blank defect trend at 23nm solidly in single-digit range, making mitigation effective for some levels

Still need engineering work to define blank fiducial strategy compatible with low defects and placement accuracy

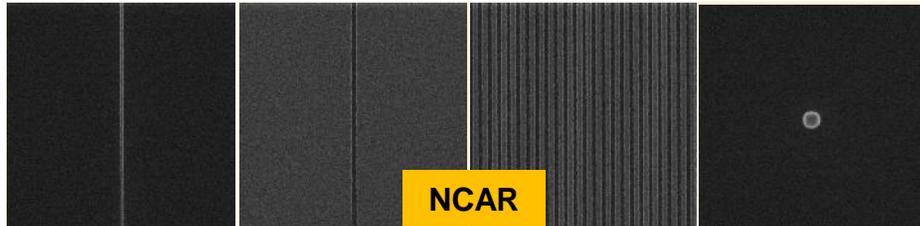
EUV FRONT END MASK MAKING IS ACHIEVABLE

Isolated Line		Isolated Space		Dense L/S		Isolated Contact	
Design	Actual	Design	Actual	Design	Actual	Design	Actual
50nm	55.2nm	40nm	31.8nm	40nm	35.6nm	50nm	32.1nm

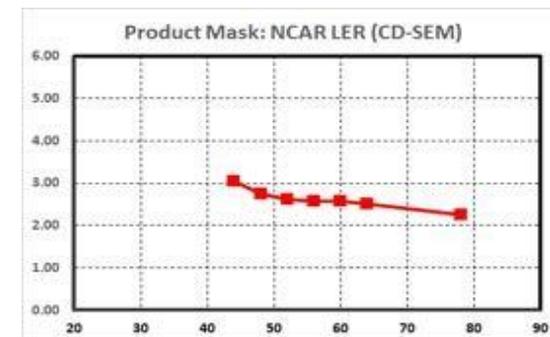
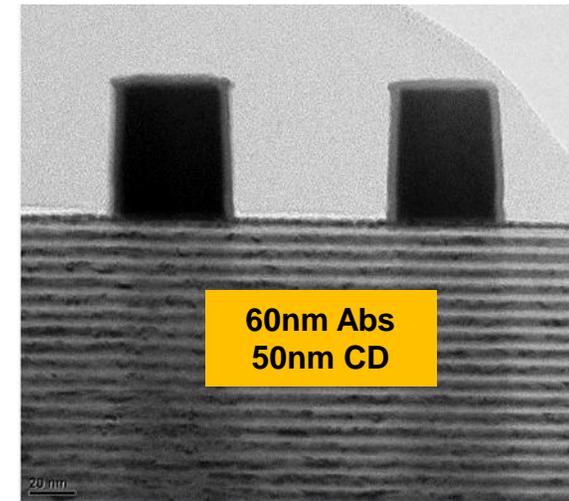


PCAR

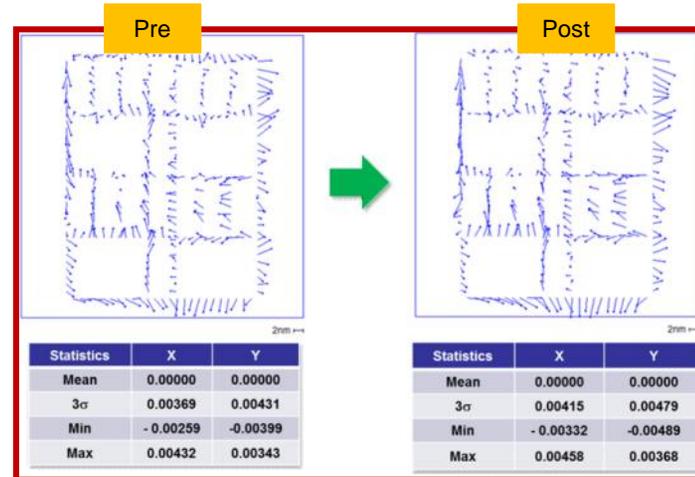
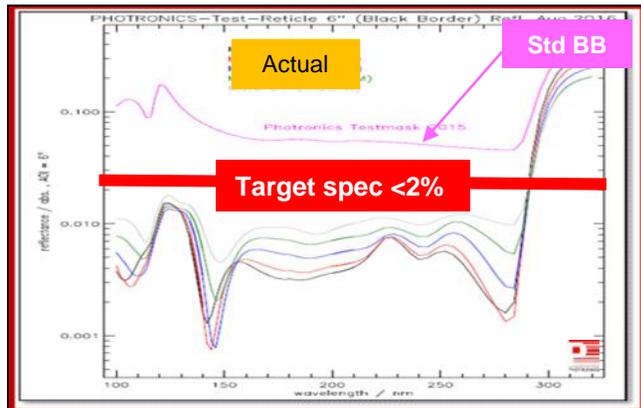
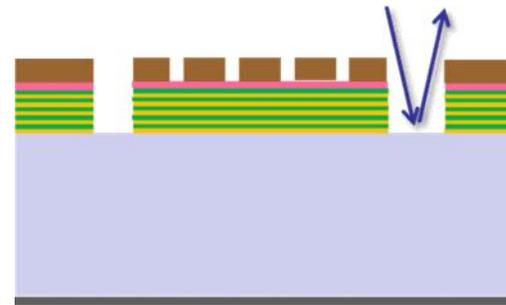
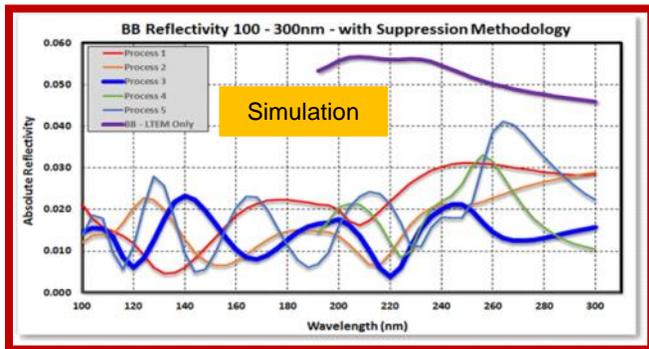
Isolated Line		Isolated Space		Dense Line		Isolated Dot	
Design	Actual	Design	Actual	Design	Actual	Design	Actual
30nm	41.6nm	50nm	43.6nm	50nm	40.2nm	60nm	66.1nm



NCAR



IMPACT OF BLACK BORDER ON OOB AND REG



LOOKING AT EUV INFRASTRUCTURE

SEMATECH EMI launched AIMS program in 2012

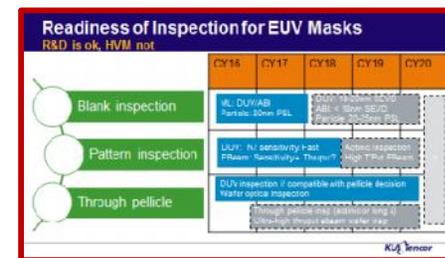
- 1st tool under installation
- Multiple companies participating

EIDEC ABI program launched in 2011

- In regular use, allows sampling at 20nm SEVD
- Defect location accuracy approaching 10nm target

Actinic Pattern inspection

- APMI is missing in action (MIA)
- Will it be too late if it ever arrives?



Xiong, Y., BACUS Panel 2015

WHY EUV?



COMPLEXITY OF PRODUCT DESIGN & TECH DEVELOPMENT

Three primary challenges

1. Design

- Learning double patterning (mask coloring)
- MP impacts on parasitic extraction and variation
- Implementation rules for place and route
- DRC/MRC

2. Manufacturing

- Fins with consistent height during etch
- 2D/3D structures impact on metrology and inspection

3. Cost

- Avg design cost for N28 planar ~ \$40M (+ 60% for embedded s/w and masks)
- Avg design cost for N14ff SOC ~ \$100M (+ 60% for embedded s/w and masks)
 - High End SOC ~ \$200M (+ ~\$100M)
 - Low End SOC with IP reuse ~\$60M (+ ~\$40M)

DESIGN PERSPECTIVE

N28 required ~100 Engineer Years to bring out design

- Team of 50 engineers 2 years to complete design to tapeout
 - + ~9-12 months for proto, test and qual
- Typical design is 11-Metal process with ~ 52 masks
 - @80% fab utilization mfg cost ~\$3500 / 300mm wafer
 - @ ~1.3 layers / day, cycle time ~70 days (min 2.5 months from start to delivery)

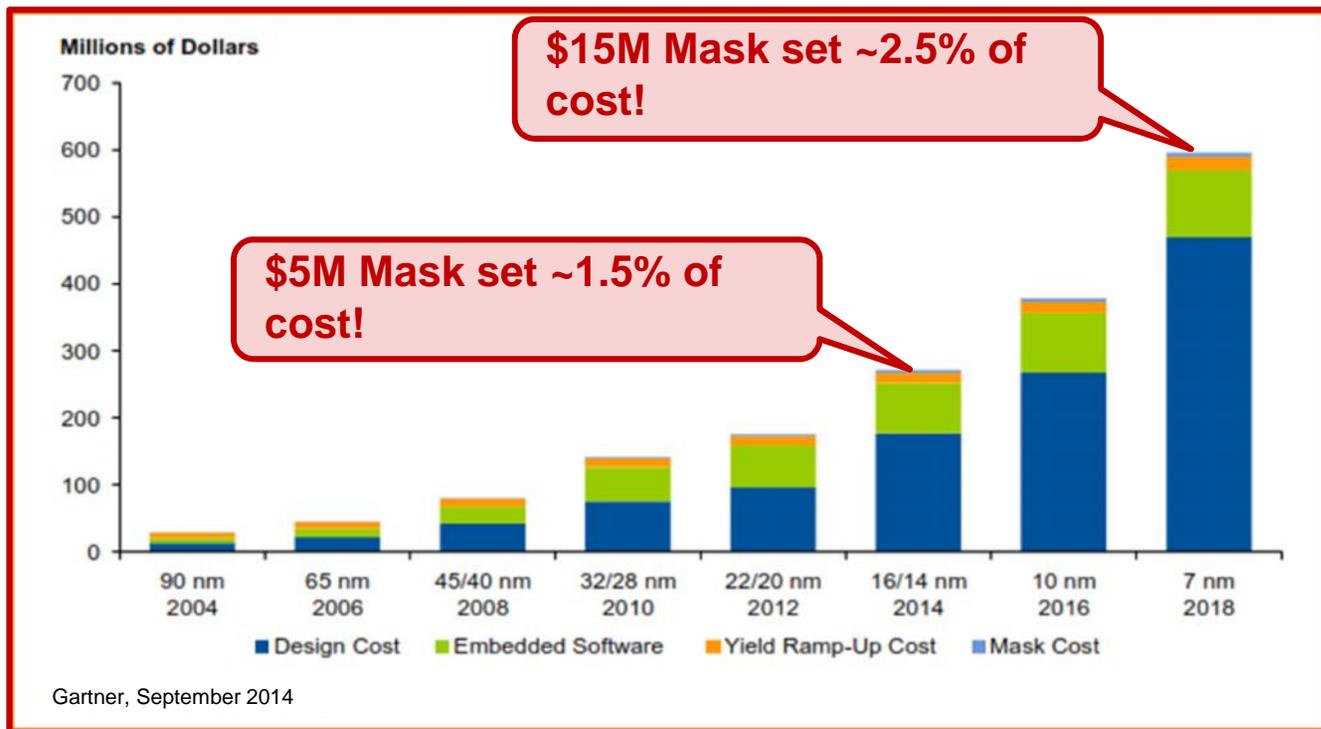
N14 required ~200 Engineer Years to bring out design

- Team of 50 engineers 4 years to complete design to tapeout
 - + ~9-12 months for proto, test and qual
- Typical design is 11-Metal process with 66 masks
 - @80% fab utilization mfg cost ~\$4800 / 300mm wafer
 - @ 1.3 layers / day, cycle time is ~90 days (min 3 months from start to delivery)

N7 early projections ~300 Engineer Years

- Team of 50 engineers 6 years to complete design to tapeout
 - + ~9-12 months for proto, test and qual
- Typical design is 11-Metal process with >80 masks (optical only)
 - NCAR processing on BEOL, low pattern density
 - LELELE or SAQP are options

DESIGN COST FOR SOC



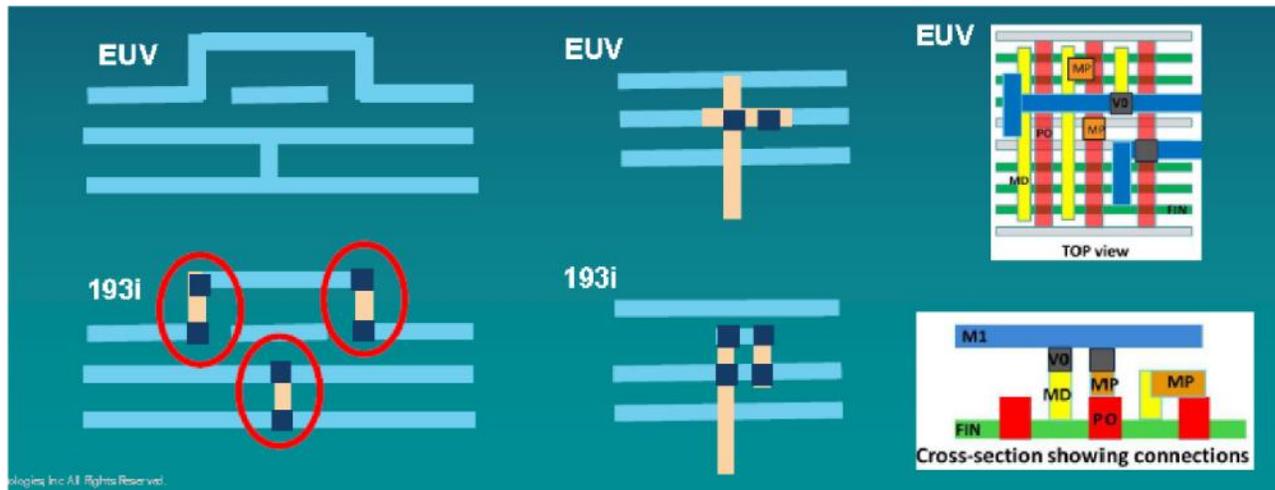
EUV: DESIGN SIMPLIFICATION

POTENTIALLY BETTER YIELD

Able to employ jogs
Reduced # vias (better yield)
Less min. length (area) wires
Able to connect to neighbor wire

Better freedom for
redundant via insertion

Reduced MOL
complexity by 2D M1



Esin Terzioglu, Qualcomm, 2014 EUVL

EUV POTENTIAL DESIGN BENEFITS IN N7

Reduced wafer/die cost due to reduced mask count and better shrink

- Reducing MOL complexity by using 2D M1 routing – **Is 2D back in vogue?**
- Replacing repetitive litho/dep/etch steps with ArF

Potential yield gains

- Reduced mask count
- Reduced number of required vias, more redundancy

Potential area gains due to less restrictions in layout

- Aggressive pitch scaling to improve die cost by area scaling
- Chance to put more functionality in the same area

EUV ON THE CUSP?

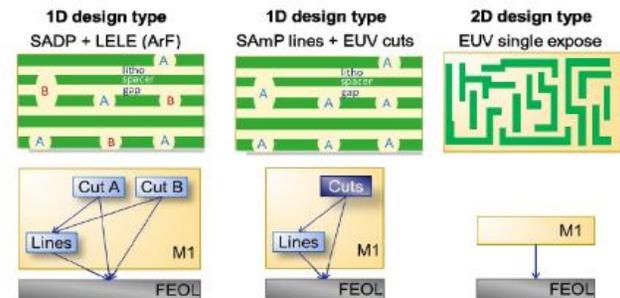
>20 NXE3400 systems forecasted for delivery in 2017/18, HVM 2019?

- > 1M wafers exposed on NXE33xx systems



Technical and Economic Drivers for adoption

- EPE, ability to keep all cuts on one layer
- Reconsider 2D layouts with SE
- 3:1 ArF:EUV cost ratio is the industry target



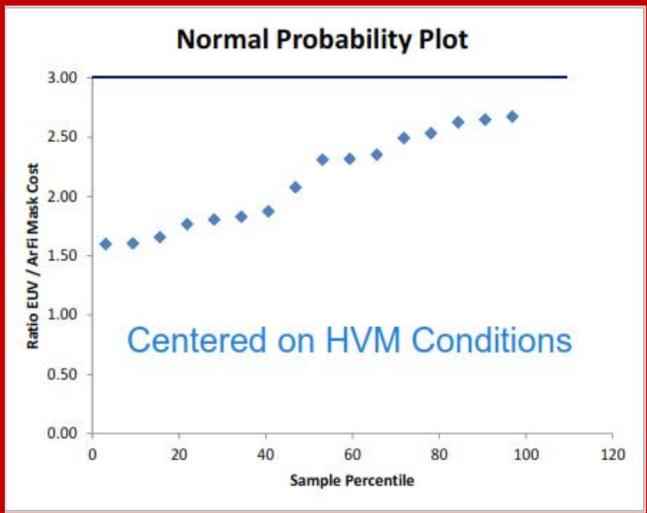
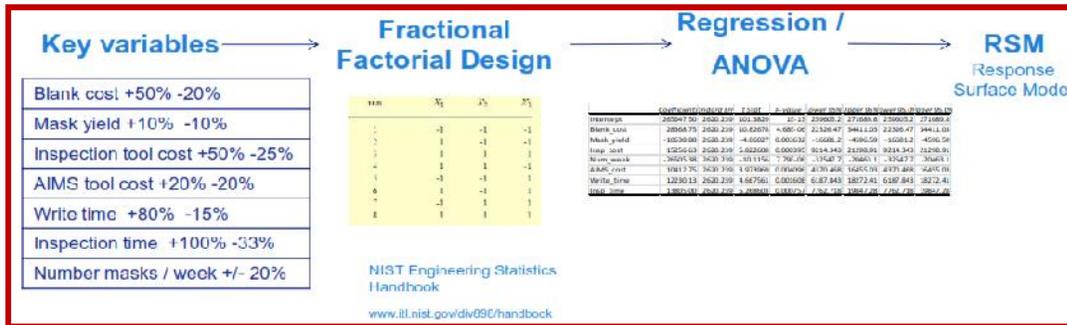
Mulkens, J., Proc. SPIE 9422, EUV Lithography2015



IMPORTANCE OF EUV MASK COST ON ADOPTION

General industry consensus:

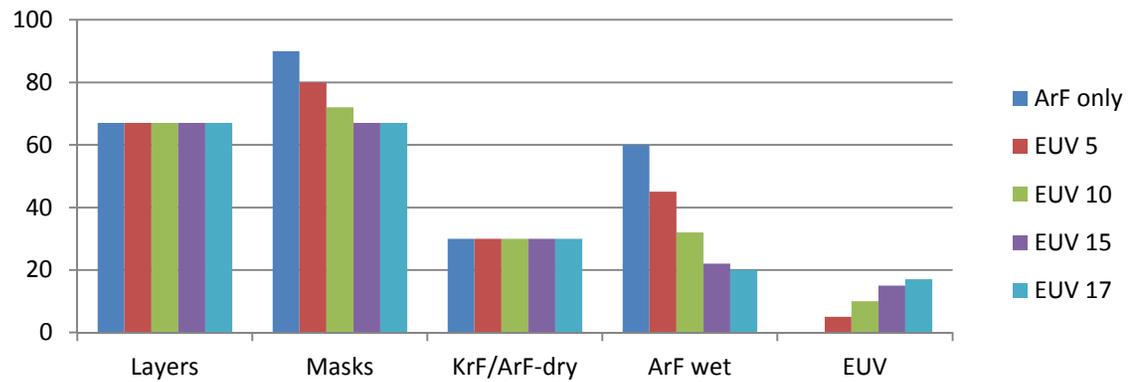
- Cost of EUV mask \leq Cost of 3x ArFi masks



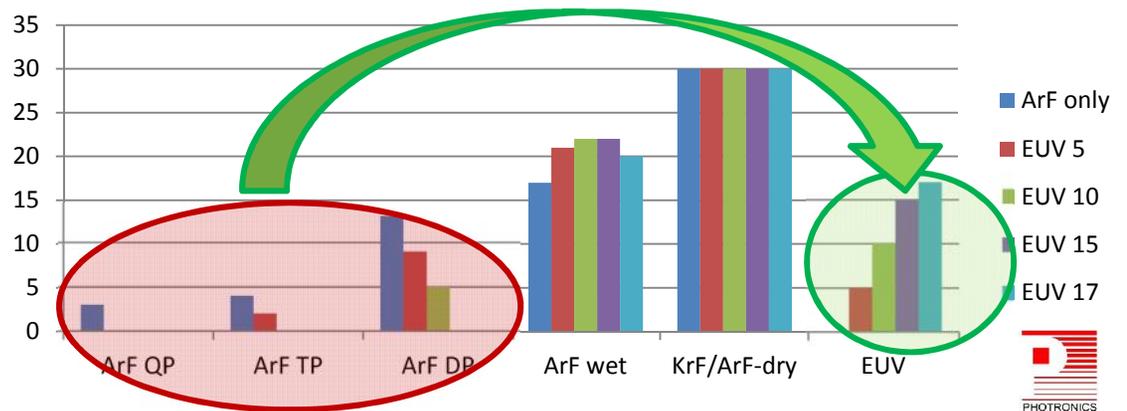
Lercel, M. Proc. SPIE 9985, Photomask Technology 2016

COST MODEL ASSUMPTIONS

Mask set make-up for 7nm node

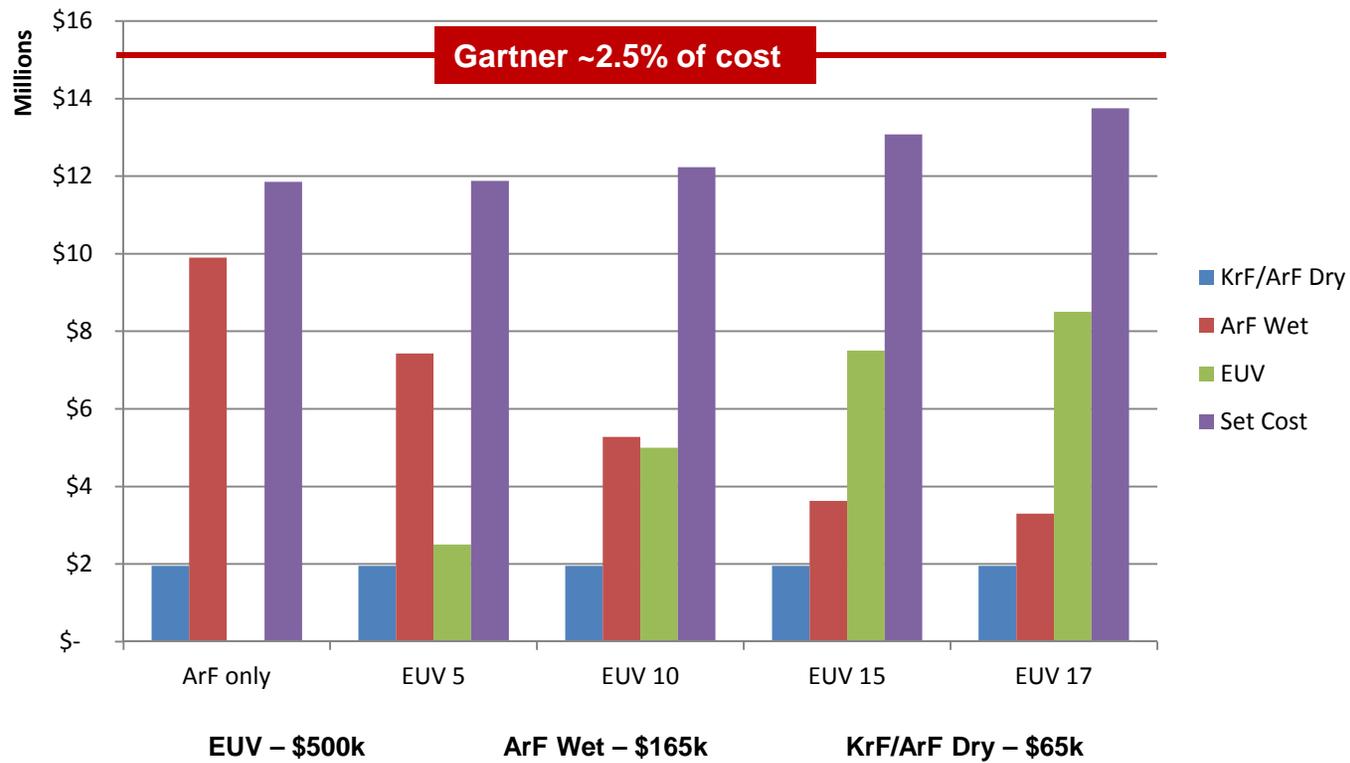


Compared multiple patterning scenarios



MASK SET COST FOR 67 LAYERS

7NM NODE



EQUIPMENT ASSUMPTIONS

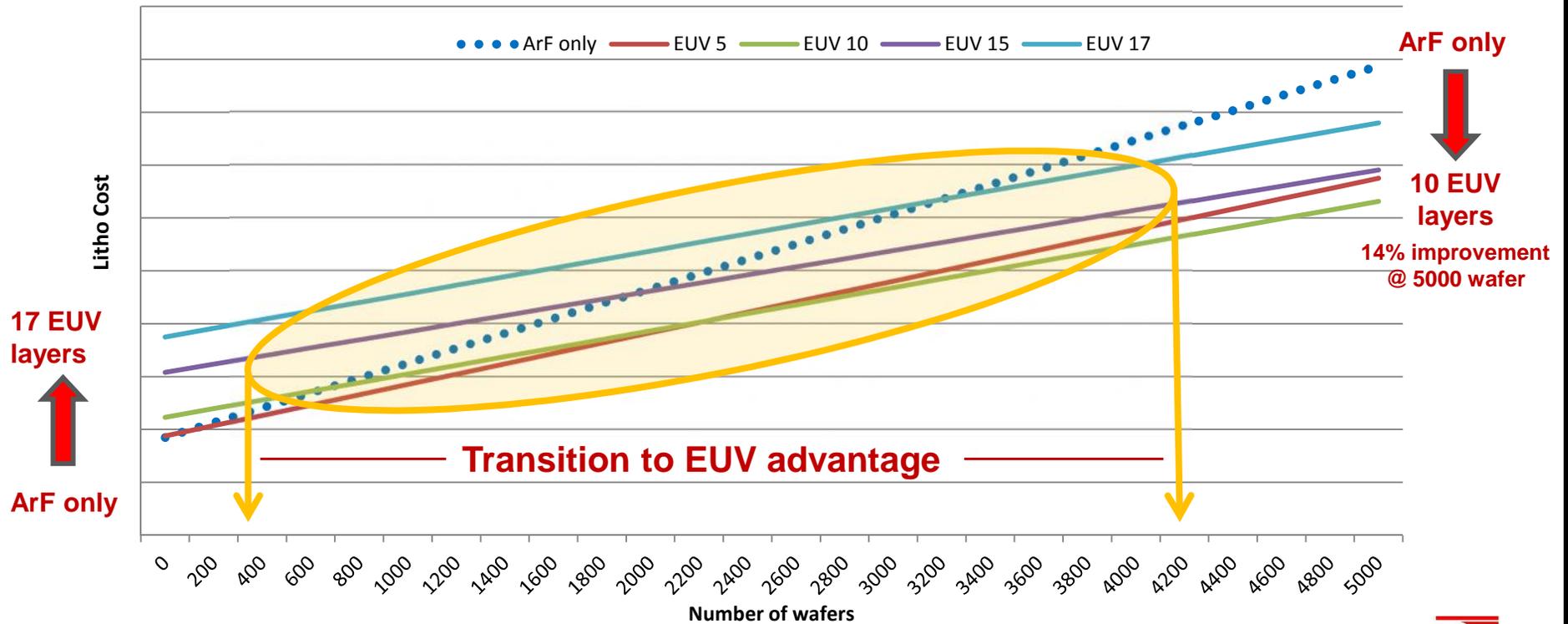
Equipment Cost

	ArF Wet	EUV	KrF/ArF Dry	Incremental	Mask
Scanner cost	\$70,000,000	\$120,000,000	\$45,000,000	\$60,000,000	\$150,000,000
Depreciation/yr	\$14,000,000	\$24,000,000	\$9,000,000	\$12,000,000	\$21,000,000
Uptime	90%	75%	90%	90%	90%
Cost/hr	\$1,776	\$3,653	\$1,142	\$1,522	\$2,718

Throughput based on patterning scenario

Strategy	PPH
ArF Wet QP	61
ArF Wet TP	81
ArF Wet DP	119
ArF Wet	250
ArF/KrF Dry	200
EUV	125

COST EFFECTIVE EUV LITHO

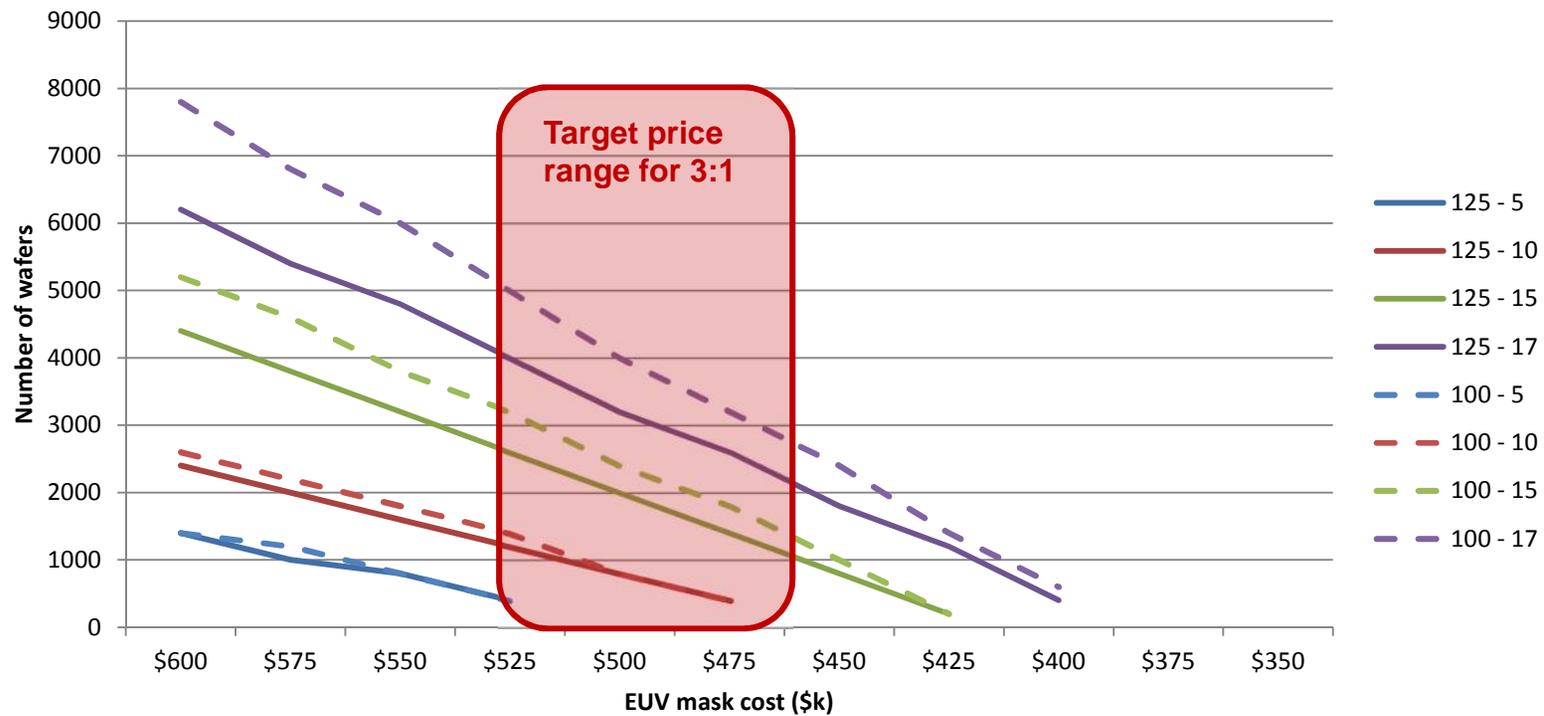


Increasing use of EUV improves cost!



COST PARITY

IMPACT OF EUV THROUGHPUT



COST PARITY

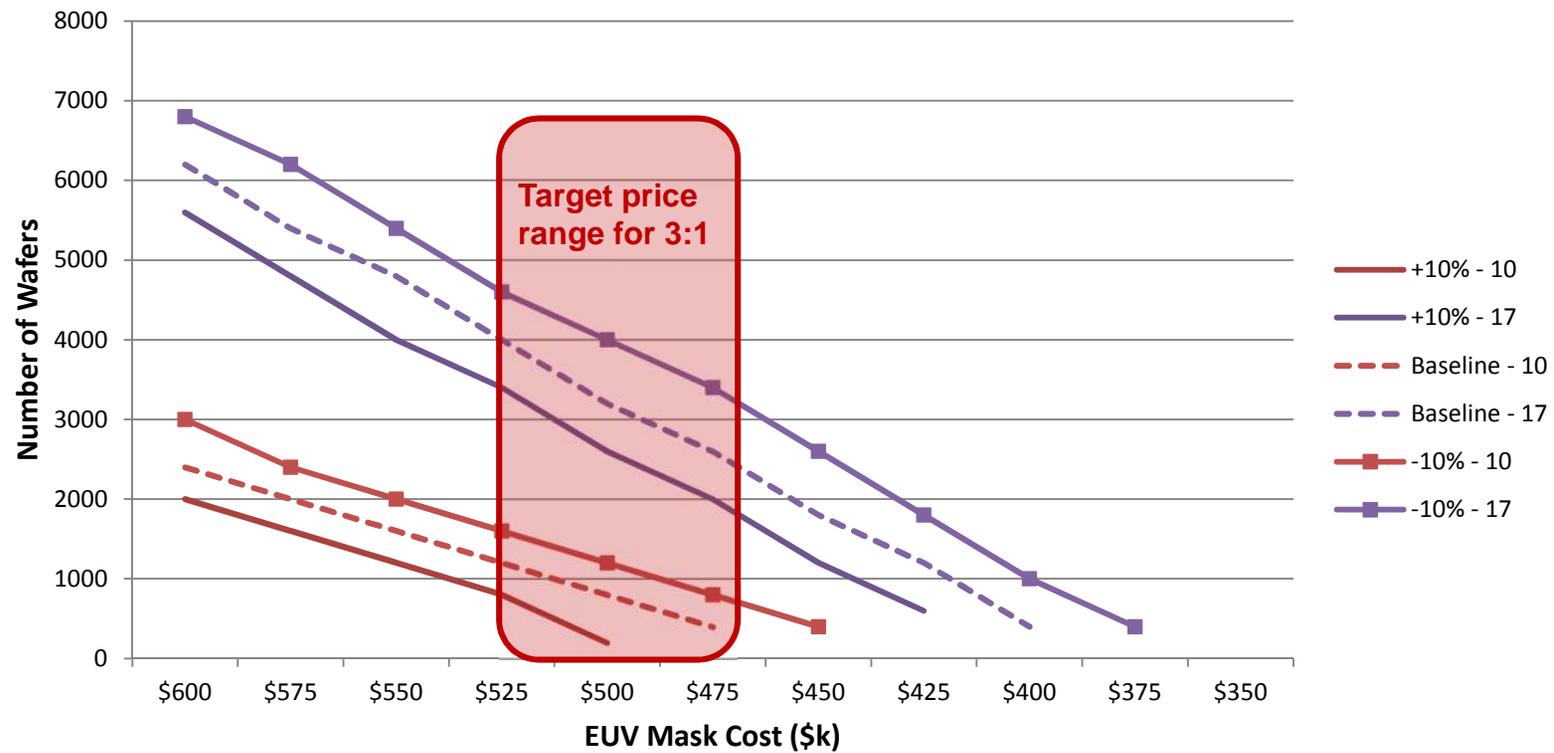
IMPACT OF OPTICAL THROUGHPUT



- **10% reduction in throughput reduces number of wafers to reach parity**
- **EUV becomes a more attractive option**

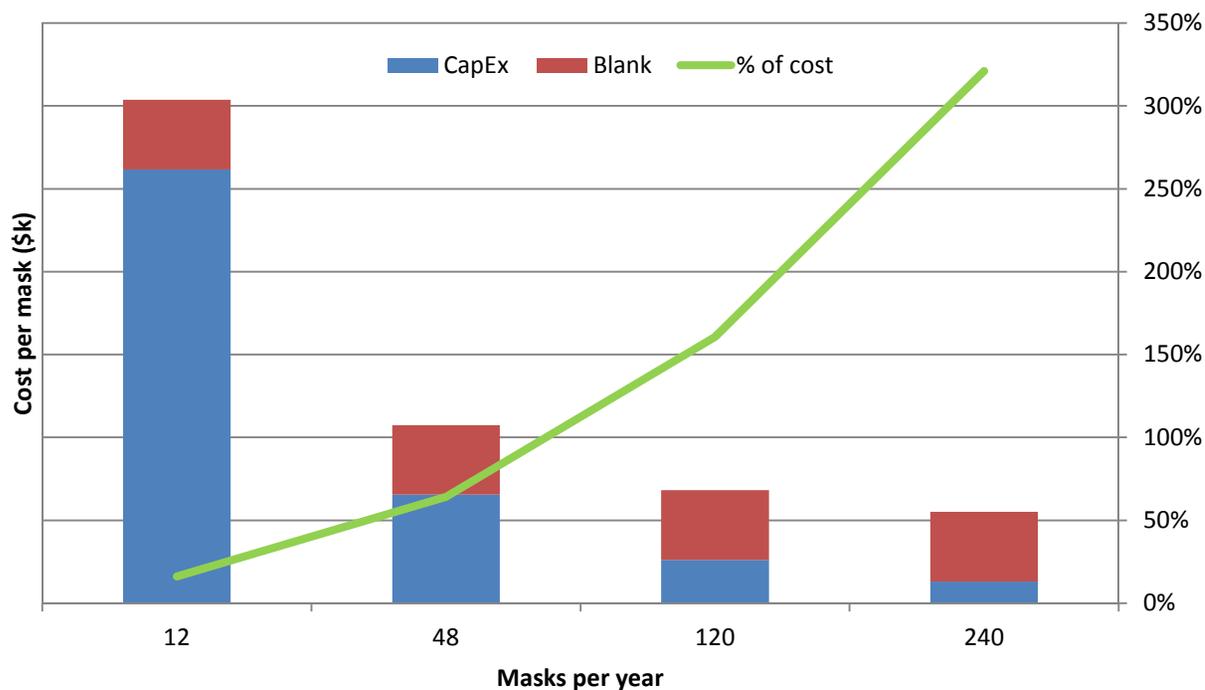
COST PARITY

IMPACT OF OPTICAL MASK COST



EUV MASK COST DRIVERS

CAPEX DEPRECIATION AND BLANK



- **CapEx investments dominate early cost**
- **As volumes increase, cost of blanks will take over**
- Does not include process yield or blank inspection (ABI)

REMAINING KEY ISSUES LIST SUMMARY

Continuous improvement on actinic inspection tools

- ABI already bearing fruit; AIMS getting started

Pattern mask inspection is a game changer for EUV

- EBMI is showing progress though speed improvements are required
- Innovate equipment and processes to allow for use with 193nm masks
- APMI is late and will be expensive but worth the costs for pattern and post pellicle inspection – who will step up to support?

Yield and Utilization are primary factors in reducing product cost

- Need critical mass to foster quality learning cycles, maximize use
- End user commitment to mask output is key for model

SUMMARY

Masks are key to the success of EUV - Significant improvements made

- Mask manufacturing is maturing, approaching HVM readiness, BEOL focus
- Blank defect reduction is required to help improve mitigation process
- Infrastructure showing progress – ABI is good benchmark for success, AIMS in early stages in the field, APMI needed but lacks owner

EUV can be cost competitive to ArF with modest scanner throughput

- Cost model validates cost parity between one EUV mask and three high-end ArFi masks
- Reverses scaling trends, improves chip density; should allow for more chips/field and reduce cost

Modest EUV volumes are required to manage EUV Mask cost

- Earlier adoption will help drive crossover from ArF multi-patterning
- **Blank cost** is largest driver for HVM



ACKNOWLEDGMENTS

Henry Kamberian and the Photronics Nanofab team

Michael Lercel - ASML

THANK YOU

